Design of a compact 200 W DC/DC converter

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Bachelorthesis – 15th of march 2017

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TECHNISCHE
UNIVERSITÄT
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Studienrichtung: Datentechnik

Bachelorthesis: Design of a compact 200 W DC/DC converter
BA 1446-16
Eingereicht: 15th of march 2017

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Abstract

This project focuses the construction of an ultra thin laptop power supply, that fits into the DVD-drive media bay. The height of the device will be limited to 1.2 cm, which is partly fulfilled by the developed prototype. Such compact power supplies require high efficiency to be passively cooled. The basic DC/DC-converter of the power supply is designed, built and tested in this work by using a series resonant half bridge topology for getting high efficiency. The SRC works sub-resonantly but with zero voltage switching provided by the transformer's main inductance current.
For analytic consideration of the SRC tank circuit including this main inductance, a little program is written that helps understanding the system behaviour.

Keywords: Switching-mode power supply, compact design, series resonant converter, laptop SMPS, DC/DC converter

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Abbreviations

abbreviation	description
AC	**A**lternating **C**urrent also used for alternating voltages
AWG	**A**merican **W**ire **G**auge
DC	**D**irect **C**urrent also used for constant voltages
EFD	**E**conomical **F**lat **D**esign transformer cores that are designed to be flat
EMI	**E**lectro**m**agnetic **I**nterference
FSM	**F**inite-**S**tate **M**achine
GaN	**Ga**llium **N**itride is a wide-bandgap semiconductor material
GUI	**G**raphical **U**ser **I**nterface
HEMT	**H**igh **E**lectrol **M**obility **T**ransistor
HRPWM	**H**igh **R**esolution **P**ulse **W**idth **M**odulation
IC	**I**ntegrated **C**ircuit
JFET	**J**unction **F**ield-**E**ffect-**T**ransistor
LLC	Converter resonant tank circuit, consisting of two inductors (**LL**) and one capacitor (**C**)
MOSFET	**M**etal-**O**xide-**S**emiconductor **F**ield-**E**ffect-**T**ransistor
MOT	**M**inimal **O**n **T**ime - Protection of rectifier driver against runaway switching
PCB	**P**rinted **C**ircuit **B**oard
PFC	**P**ower **F**actor **C**orrection reduces harmonic oscillation in the grid current. An *active* PFC is usually a simple boost converter, that can control the input current to be sinusoidal.
SMPS	**S**witching **M**ode **P**ower **S**upply
SRC	**S**eries **R**esonant **C**onverter
ZCS	**Z**ero **C**urrent **S**witching means that there is no or just a low current flowing through the transistor when it switches off
ZVS	**Z**ero **V**oltage **S**witching means that there is no voltage on the transistor, when it switches on

Physical symbols

symbol	unit	description
C	F	capacity
f	Hz	frequency
I	A	direct current
i	A	time dependant current
L	H	inductivity
R	Ω	resistance
t	s	time
T	°C	temperature
V	V	voltage
v	V	time dependant voltage
τ	s	period duration
ω	Hz	angular frequency

Circuit symbols and indices

index	description
AMP	amplifier / linear controller
C	capacitor
D	diode / rectifier
DRV	gate driver
F	Fuse
g	gate (usually to ground)
GS	gate - source
h	main inductance
in	input
L	inductor / transformer
out	output
pri	primary side
Q / q	transistor or transistor parasitic element
R	resistor
res	resonant element
SD	source - drain
sec (sometimes just s)	secondary side
U / u	voltage converter
V	voltage supply / voltage source
σ	stray inductance / resistance

1 Introduction

1.1 Motivation

Miniaturisation is an ongoing trend for nearly all types of mobile devices. Laptops became thinner and lighter or, when regarding workstation laptops, the amount of power and additional equipment was increased. But laptops with internal power supply disappeared from the market. For laptops having 90 W power or less, very small, external power supplies are available but the size of the power supplies immediately increases when going to 120 W or more. This project analyses the ability of constructing an ultra thin power supply that fits in the DVD-drive media bay of a laptop and can handle 200 W for powerful workstation or gaming laptops.
A prototype of the basic DC-DC-Converter stage is constructed.

1.2 Requirements

The most important requirement for this power supply is to be compact. But simply using a topology with low number of parts will not work: The amount of heat, that can be dissipated to the environment is limited by the total surface of the device. The surface temperature may not become higher than 60°C. This power supply should also work in the media bay of a laptop. When dissipating more than 10 W of heat into this bay, some other laptop components can overheat, as been shown in corresponding work. [7] Converting a total output power of 200 W with 10 W of power loss corresponds to an efficiency of 95.2 % for the maximum power point.

The effective volume (excluding case and indentations) for the PCB board is $10\,\text{mm} \times 125\,\text{mm} \times 100\,\text{mm} = 112.5\,\text{cm}^3$. So the power density of transformation has to be $1.78\,\frac{\text{W}}{\text{cm}^3}$. There are cheap laptop power supplies heaving 90 W @ $1.36\,\frac{\text{W}}{\text{cm}^3}$ and about 90 % efficiency on the market. These devices apparently are using active PFCs, that converts 100..250 V AC to 380 V DC and then a half bridge topology to convert to 19.5 V DC, operating at 125 kHz and with active rectification having two secondary windings (centre tab) on the output side. [7]

For this project, a SRC is going to be used instead of the simple half bridge. To achive the higher power density and efficiency, an increase of the switching frequency and the use of modern GaN HEMTs is intended.

Table 1.1.: Target design parameters

output voltage	19.5 V
output power	200 W
input voltage	380 V DC
switching frequency	200 kHz; tends to become higher
maximum power loss	10 W in the complete device - maybe 6 W in this DC/DC-Converter
topology	SRC (series resonant converter)

Some elements on the PCB have been changed on several times during the development. Two complete PCBs were soldered. The different revisions of the device are marked with hashtags #. The changes between the revisions are explained in section 5.1.

1.3 Topology

The decision of building a half bridge was made in previous work. But there are still a lot of parameters to be chosen. The output voltage on this kind of SMPS is regulated by using an active PFC, that can boost the grid voltage. Therefore the primary switching voltage is between 380 and 400 V. It is also possible to use a buck-boost-converter for the PFC and have a lower switching voltage. But there is one more Transistor in the power path of the buck-boost-converter so there cannot be a large efficiency benefit. Currently marketable GaN-transistors are designed for 650 V. This blocking voltage is even more than 1.5 times larger than the switching voltage and the use of reduced switching voltage were a bad idea. On the regarded prototype there will be no PFC and no voltage control, the output voltage will not exactly be 19.5 V.
When using the PFC for voltage control, the transformer stage is not unregulated. The SRC should be able to do a current control for buffering the 50 Hz power leaks that cause a certain voltage breakdown in the primary capacitor(s). It depends on this flow control range of the SRC and the target life period of the power supply, how large the capacitor C_1 has to be. This capacitor has significant influence on the total size of the device.
The size of most other capacitors and coils shrinks with increasing switching frequency.

2 Analysis

2.1 Mathematical model of single half bridge series resonant converters

The SRC circuit, completely transformed to the primary side, looks as follows:

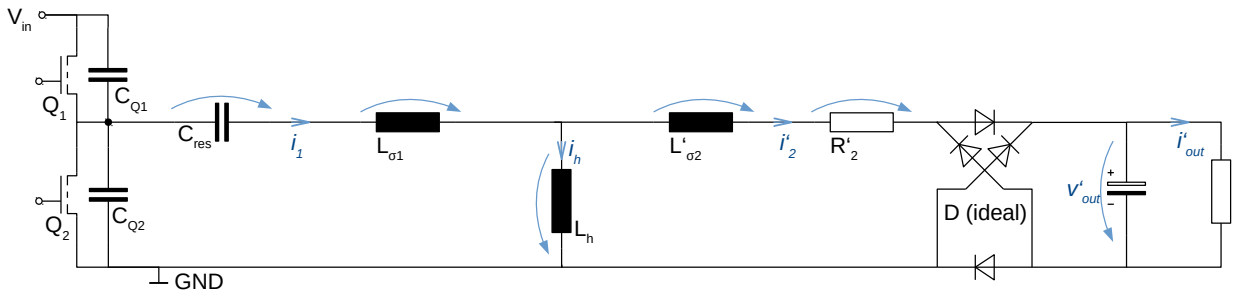


Figure 2.1.: Real transformer model of SRC circuit

The capacitor C_{res} is not just there for the resonance; it also blocks DC currents that would drive the transformer into saturation. In quasi-stationary operation, the DC part of the voltage has to be $V_{\text{Cres,DC}} = \frac{V_{\text{in}}}{2}$. The transistors Q_1 and Q_2 have to be turned on for the same duration during one period ($t_1 - t_0 = t_3 - t_2$), otherwise $V_{\text{Cres,DC}}$ would change and the rectified voltage pulses on the secondary side had different values. Therefore the current would not spread equally over all pulses. Upon reversion, a duty cycle $\neq 0.5$ can be used to compensate a diversity of current pulses that is caused for example by PCB asymmetry. More in section 4.1.1. For theoretical consideration the system can be assumed to be symmetrical.

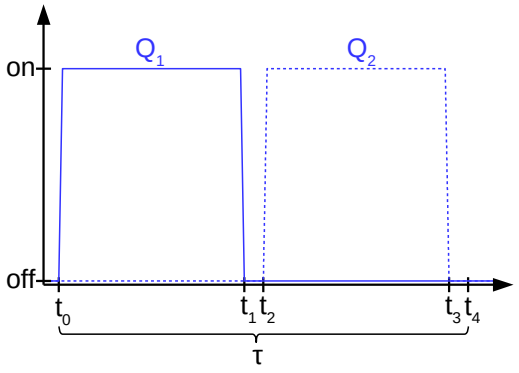


Figure 2.2.: Period sequences

For analysis the output capacitor C'_{out} is assumed to be large enough, that $V_{\text{C'out}}$ is constant over one period τ. For the first interval $(t_0..t_1)$ of τ two cases have to be taken into account separately:

2.1.1 Case open: diode rectifier blocking (t_0 .. t_1)

In this case $i_1 = i_h$ and $V_{in} = V_{Lh} + V_{L\sigma 1} + V_{Cres} = (L_h + L_{\sigma 1}) \cdot \frac{\delta i_1}{\delta t} + \int \frac{i_1 \delta t}{C_{res}}$. The solution for this differential equation can easily be written as:

$$i_h = a \cdot \sin(\omega t) + b \cdot \cos(\omega t) \quad \text{with} \quad \begin{array}{rcl} \omega & = & \frac{1}{\sqrt{C_{res} \cdot (L_{\sigma 1} + L_h)}} \\ a & = & (V_{in} - V_{Cres,0}) \cdot \sqrt{\frac{C_{res}}{L_{\sigma 1} + L_h}} \\ b & = & i_{h,0} \end{array} \tag{2.1}$$

2.1.2 Case short: diode rectifier conducting (t_0 .. t_1)

This case is much more complicated. It applies $i_1 = i_h + i_2$, $V_{in} = V_{Lh} + V_{L\sigma 1} + V_{Cres}$ and $V_{Lh} = V_{C'out} + V_{R'2} + V_{L'\sigma 2}$. From this, a system of two linear differential equations can be derived:

$$\begin{array}{rcl} L_h \cdot \frac{\delta i_h}{\delta t} & = & V_{C'out} + i_2 \cdot R'_2 + L'_{\sigma 2} \cdot \frac{\delta i_2}{\delta t} \\ V_{in} & = & L_h \cdot \frac{\delta i_h}{\delta t} + L_{\sigma 1} \frac{\delta (i_h + i_2)}{\delta t} + \int \frac{i_h + i_2}{C_{res}} \delta t \end{array} \tag{2.2}$$

The characteristical polynom

$$A\omega^4 + B\omega^3 + C\omega^2 + D\omega = 0 \quad \text{with} \quad \begin{array}{rcl} A & = & C_{res} \cdot (L_h L_{\sigma 1} + L_h L'_{\sigma 2} + L_{\sigma 1} L'_{\sigma 2}) \\ B & = & C_{res} R'_2 \cdot (L_h + L_{\sigma 1}) \\ C & = & L_h + L'_{\sigma 2} \\ D & = & R'_2 \end{array} \tag{2.3}$$

has the trivial solution, one real solution and two complex ones, assuming, that the system works above the aperiodic boundary case. All currents (i_1, i_h and i_2) have the scheme

$$i_* = a_* \cdot e^{\beta_1 t} + (b_* \cdot sin(\omega t) + c_* \cdot cos(\omega t)) \cdot e^{\beta_2 t} + d_* \tag{2.4}$$

with different factors a_*, b_*, c_*, d_* but equal oscillation and damping constants, which are given with:

$$\begin{array}{rcl} \omega & = & \frac{\sqrt{3}}{2}(u + v) \\ \beta_1 & = & u + v - \frac{B}{3A} \\ \beta_2 & = & -\frac{B}{3A} - \frac{1}{2}(u + v) \end{array} \quad \text{where} \quad \begin{array}{rcl} u & = & \sqrt[3]{-\frac{q}{2} + \sqrt{\frac{q^2}{4} + \frac{p^3}{27}}} \\ v & = & \sqrt[3]{-\frac{q}{2} - \sqrt{\frac{q^2}{4} + \frac{p^3}{27}}} \end{array} \quad \begin{array}{rcl} p & = & \frac{9AC - 3B^2}{9A} \\ q & = & \frac{2B^3 - 9ABC + 27A^2 D}{27A^3} \end{array} \tag{2.5}$$

The relations of the three currents are

$$\begin{array}{rcl} i_1 & = & i_h + i_2 \\ i_h & = & \frac{1}{L_h} \cdot \int \left(V_{C'out} + R'_2 i_2 + L'_{\sigma 2} \cdot \frac{\delta i_2}{\delta t} \right) \delta t \end{array} \tag{2.6}$$

The second of these equations can be integrated and brought to the scheme 2.4. This implies relations between the factors a_2, b_2, c_2, d_2 and a_h, b_h, c_h, d_h:

$$\begin{aligned} a_\mathrm{h} &= a_2 \cdot \left(\frac{R'_2}{\beta_1 L_\mathrm{h}} + \frac{L'_{\sigma 2}}{L_\mathrm{h}} \right) \\ b_\mathrm{h} &= \frac{L'_{\sigma 2} b_2}{L_\mathrm{h}} + \frac{R'_2 b_2 \beta_2 + R'_2 c_2 \omega}{L_\mathrm{h} \cdot (\beta_2^2 + \omega^2)} \\ c_\mathrm{h} &= \frac{L'_{\sigma 2} c_2}{L_\mathrm{h}} + \frac{R'_2 c_2 \beta_2 - R'_2 b_2 \omega}{L_\mathrm{h} \cdot (\beta_2^2 + \omega^2)} \end{aligned} \tag{2.7}$$

Because the capacitor C_res blocks direct currents, $d_1 = d_\mathrm{h} + d_2$ should be zero:

$$d_\mathrm{h} = -d_2 \tag{2.8}$$

When integrating i_h in 2.6, there is a term $\frac{d_2 R'_2 + V_{\mathrm{C'out}}}{L_\mathrm{h}} \cdot t$ in i_h, which does not fit the scheme 2.4 and should be zero. This gives $d_2 = -\frac{V_{\mathrm{C'out}}}{R'_2}$. When assuming that the rectifier is always shorted and the output voltage is fixed, then this d_2 was the maximum current, that can flow from the output capacitor through the secondary side path.
Two more factors can be derived from the currents at t = 0:

$$\begin{aligned} & i_2(t=0) := i_{2,0} \\ & a_2 + c_2 + d_2 = i_{2,0} \\ & a_2 = i_{2,0} - c_2 + \frac{V_{\mathrm{C'out}}}{R'_2} \end{aligned} \tag{2.9}$$

$$\begin{aligned} & i_\mathrm{h}(t=0) := i_{\mathrm{h},0} \\ & a_\mathrm{h} + c_\mathrm{h} + d_\mathrm{h} = i_{\mathrm{h},0} \\ & c_2 = \frac{i_{\mathrm{h},0} L_h - \frac{V_{\mathrm{C'out}}}{R'_2} \cdot \left(\frac{R'_2}{\beta_1} + L'_{\sigma 2} + L_\mathrm{h} \right) + \frac{R'_2 b_2 \omega}{\beta_2^2 + \omega^2} - i_{2,0} \cdot \left(\frac{R'_2}{\beta_1} + L'_{\sigma 2} \right)}{\frac{R'_2 \beta_2}{\beta_2^2 + \omega^2} - \frac{R'_2}{\beta_1}} \end{aligned} \tag{2.10}$$

At last, the factor b_2 has to be determined. Therefore the second differential equation of 2.2 is used at t = 0 (computational solution):

$$\begin{aligned} V_{in} = {} & (L_{\sigma 1} \cdot (a_\mathrm{h} + a_2) + L_h a_h) \cdot \beta_1 + L_\mathrm{h} \cdot (b_\mathrm{h} \omega + c_\mathrm{h} \beta_2) + L_{\sigma 1} \cdot ((b_h + b_2) \cdot \omega + (c_\mathrm{h} + c_2) \cdot \beta_2) + V_{\mathrm{Cres},0} \\ b_2 = {} & -(L_\mathrm{h}^2 \cdot \beta_1 \cdot (L_{\sigma 1} + L'_{\sigma 2}) \cdot (\beta_1 - \beta_2) \cdot (\beta_2^2 + \omega^2) \cdot (R'_2 \cdot i_{\mathrm{h},0} - V_{\mathrm{C'out}}) \\ & - L_\mathrm{h} \cdot (L_{\sigma 1} \cdot (L'_{\sigma 2} \cdot \beta_1 \cdot (\beta_1 - \beta_2) \cdot (\beta_2^2 + \omega^2) \cdot (R'_2 \cdot (i_{2,0} - i_{\mathrm{h},0}) + 2 \cdot V_{\mathrm{C'out}}) \\ & + R'_2 \cdot \beta_2 \cdot (\beta_1^2 - \beta_2^2 - \omega^2) \cdot (R'_2 \cdot i_{2,0} + V_{\mathrm{C'out}})) + L'^2_{\sigma 2} \cdot \beta_1 \cdot (\beta_1 - \beta_2) \cdot (\beta_2^2 + \omega^2) \cdot (R'_2 \cdot i_{2,0} + V_{\mathrm{C'out}}) \\ & + L'_{\sigma 2} \cdot R'_2 \cdot \beta_2 \cdot (\beta_1^2 - \beta_2^2 - \omega^2) \cdot (R'_2 \cdot i_{2,0} + V_{\mathrm{C'out}}) + R'^2_2 \cdot (R'_2 \cdot i_{2,0} + V_{\mathrm{Cres},0} - V_{\mathrm{in}} \\ & + V_{C'out}) \cdot (\beta_1 \cdot \beta_2 - \beta_2^2 - \omega^2)) - L_{\sigma 1} \cdot (L'_{\sigma 2} \cdot \beta_1 + R'_2) \cdot (L'_{\sigma 2} \cdot (\beta_1 - \beta_2) \cdot (\beta_2^2 + \omega^2) \\ & + R'_2 \cdot (\beta_1 \cdot \beta_2 - \beta_2^2 - \omega^2)) \cdot (R'_2 \cdot i_{2,0} + V_{\mathrm{C'out}})) \; / \; (R'^2_2 \cdot \omega \cdot (\beta_1^2 - 2 \cdot \beta_1 \cdot \beta_2 \\ & + \beta_2^2 + \omega^2) \cdot (L_h \cdot (L_{\sigma 1} + L'_{\sigma 2}) + L_{\sigma 1} \cdot L'_{\sigma 2})) \end{aligned} \tag{2.11}$$

The complexity of this and the other equations shows the limits of this methodology. It will be necessary to do the calculations by using computer software.

2.1.3 Other cases (t_1 .. t_4)

The rest of the period is quite simple. When Q_2 is on, just set V_{in} to 0. When both transistors are off, replace C_{res} with $\frac{C_{\text{res}}+C_{Q1}+C_{Q2}}{C_{\text{res}}\cdot(C_{Q1}+C_{Q2})}$ while carefully regarding the boundary conditions.

2.1.4 Switching conditions

For modelling the switching transistors and the flyback diodes, the transistors are assumed to have three switching states:

- block: The transistor is blocking (forward direction only)
- diode: The flyback diode is conducting (reverse direction only)
- channel: The transistor is on

The switching of the diode rectifier D is not depending on the transistors. This yields the following two finite-state machines:

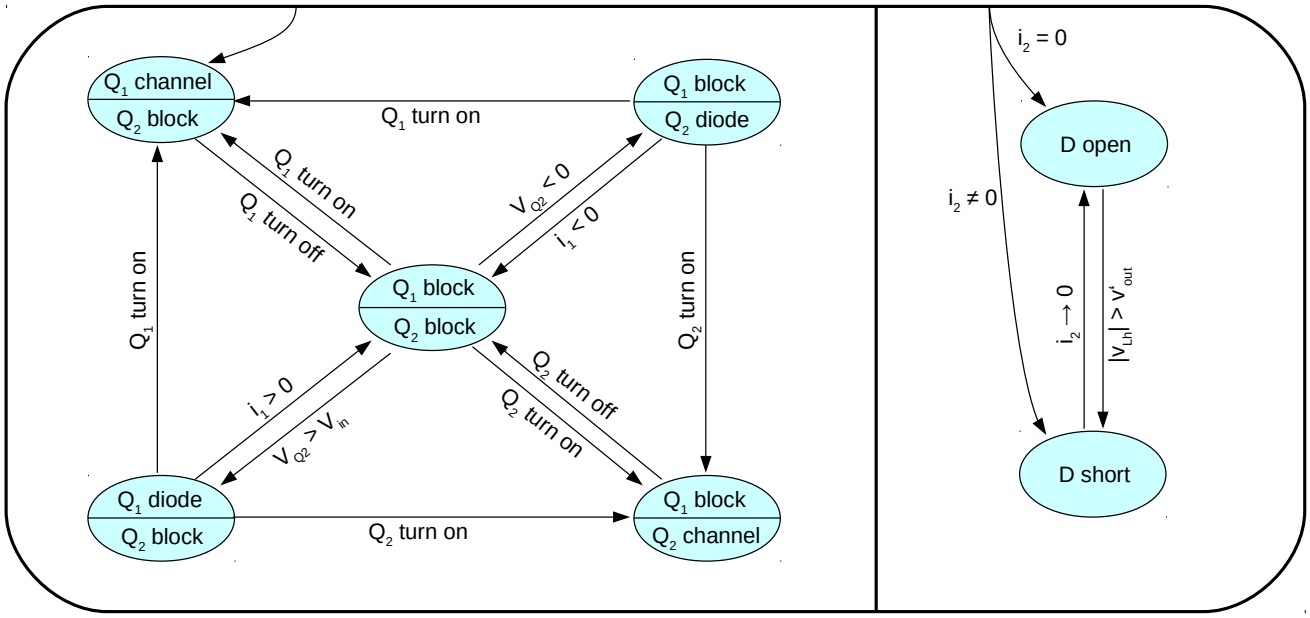


Figure 2.3.: SRC switching finite state machines

There are missing some transitions in the left FSM 2.3, for example (Q_1 channel $|Q_2$ block) $\rightarrow$ (Q_1 diode $|Q_2$ block). These transitions usually occur seldom and can be replaced by going to the central (Q_1 block $|Q_2$ block)-state and from there to (Q_1 diode $|Q_2$ block) after 0 seconds. Therefore, a check weather the transition condition is fulfilled at the beginning of a state, is required.

2.2 Program

All the equations and switching conditions from 2.1 are too complicated to be handled "by hand", so a little tool was written, that can compute the signal curves of all relevant values. As a first step, this is just an inflexible but fast circuit simulation with fixed output voltage. The benefit is, that this tool can immediately branch to the steady state and reacts fast on any change.
Usually there is a certain switching frequency intended, when designing a new SRC. It is difficult to build a transformer with exact stray inductances, so the capacitor C_{res} has to be adjusted several times during the design process. Also the dead times change with new parameters for the transformer. Therefore this tool can automatically adjust C_{res} (fig. 2.1). The user can decide, if the circuit should work over-resonant or sub-resonant. In the over-resonant case, the stray inductances are used, to (de)charge the transistor's capacitances. Therefore, a certain load current has to flow to have the zero voltage switching.
Depending on the main and stray inductances and the size (capacity) of the transistors, there may exist no fixed dead time, which can ensure zero voltage switching over all load values. In this case it is necessary to measure the output current and control the dead time. One main functionality of the tool is, to calculate the voltages and currents on the transistors in the switching moments as a function of the output current. From this graph, it can be seen, if the circuit will work with fixed dead times or if a complex control strategy is necessary. The program is intended to help also designing such control strategies or to approximate the losses of the system.
The program is meant to be public domain licensed and a little overview about the source code is documented in A.1.

2.2.1 Analytic example

For one example, typical parameters of a SRC are given to the program:

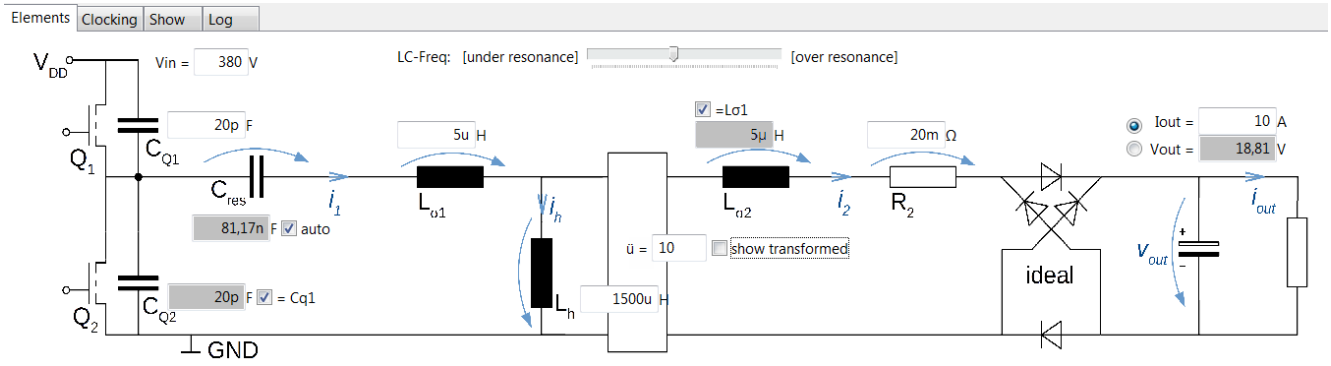


Figure 2.4.: Program: circuit elements tab

The frequency is 204 kHz:

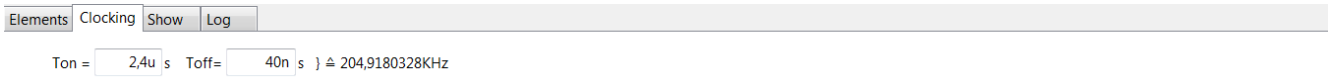


Figure 2.5.: Program: clocking tab

The program calculates the steady state signals:

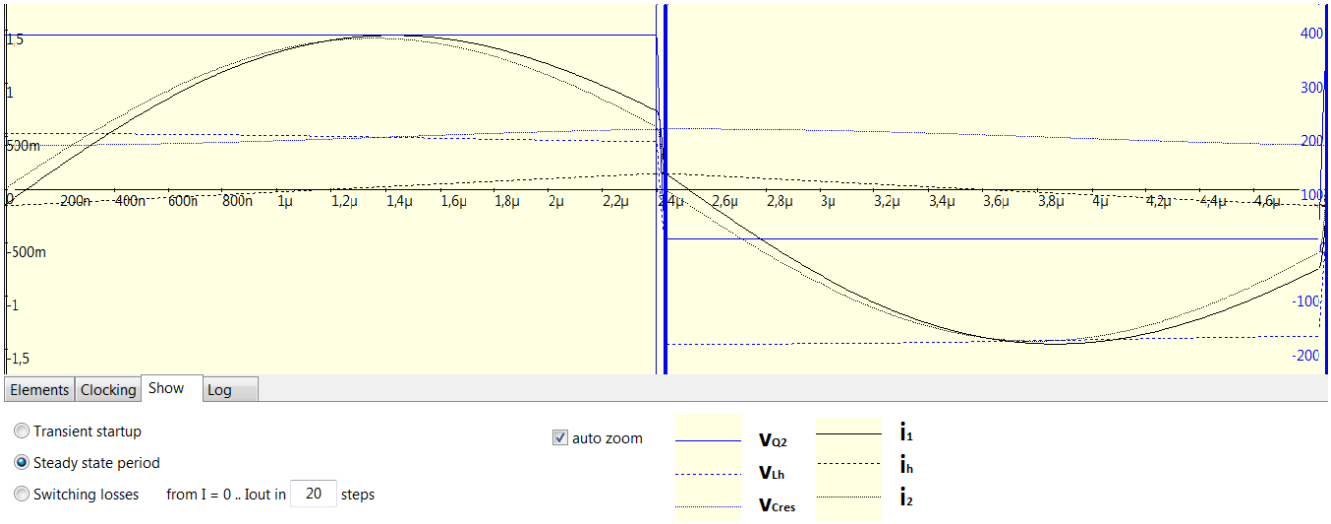


Figure 2.6.: Program: steady state period

Finally the switching currents and voltages can be calculated depending on the output current:

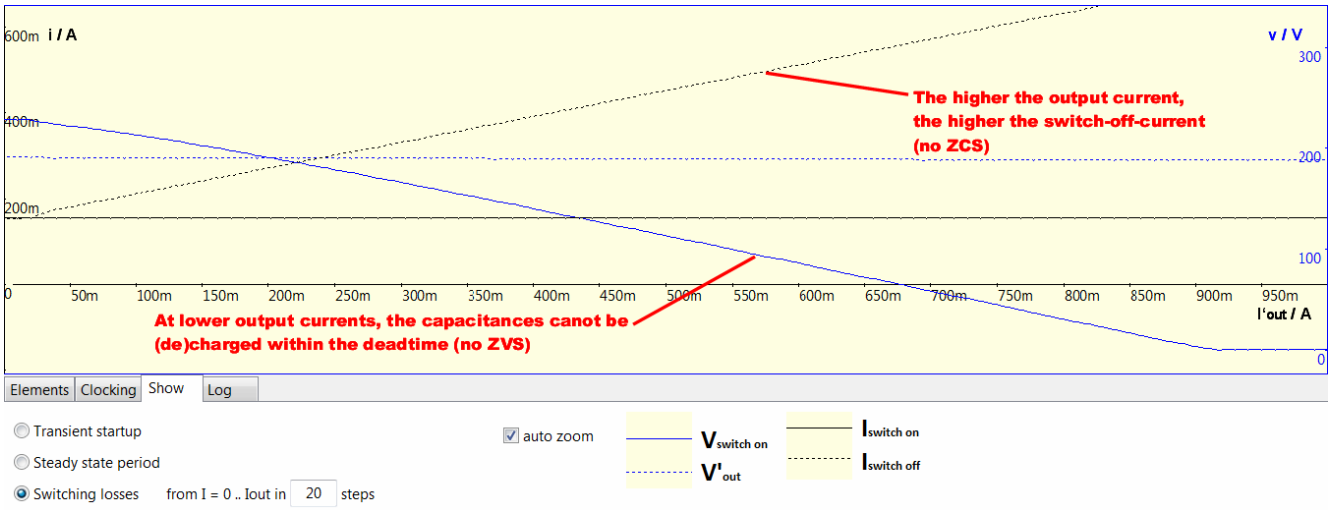


Figure 2.7.: Program: switching voltages and - currents

Figure 2.7 shows the main problem with over-resonant switching: A period and dead time duration that is optimized for the maximum load, will not provide ZVS at lower output currents. By switching

off earlier, the ZVS works for lower output currents but the switch-off-current increases. In open loop condition, there is no ZVS if the dead time gets not regulated.

2.2.2 Dead time

During the dead time, a lot of switching actions can occur. Under real conditions (non-ideal switches), the intersections between the different states are blurred, but the program marks the switching moments. For one example, a long dead time in over-resonant mode is regarded:

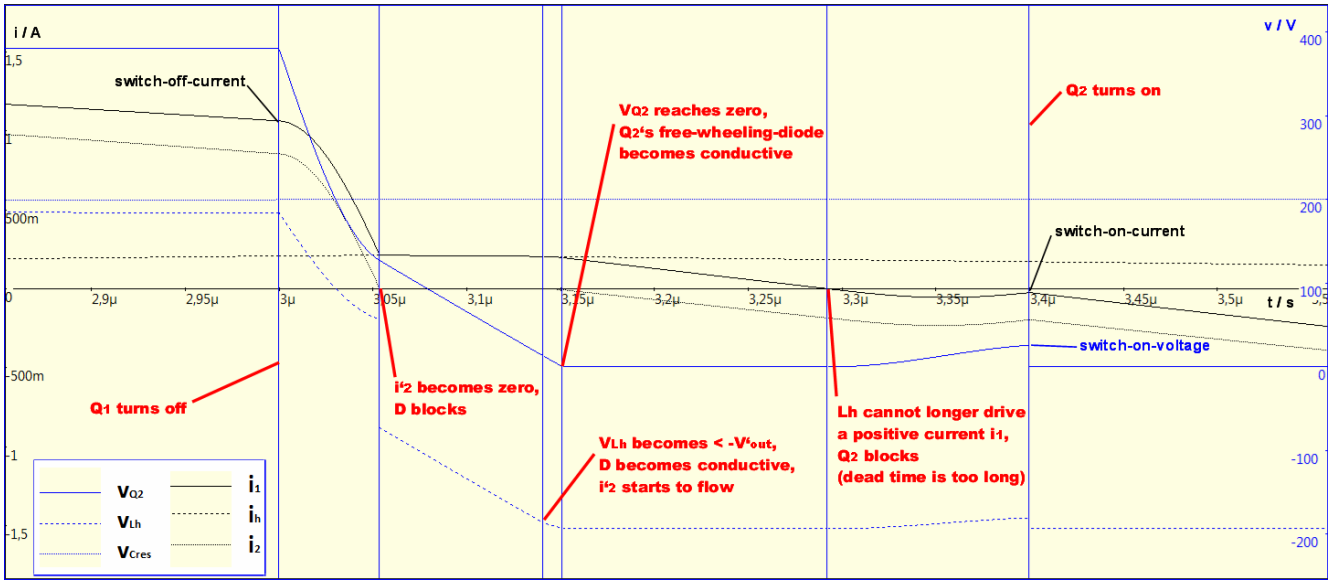


Figure 2.8.: Long dead time example

As soon as the voltage on Q_2 reaches zero, the transformer's output voltage can exceed the output voltage on C_{out}. This causes the next current pulse to start and this current gets subtracted from the main inductance current and causes i_1 to become negative.

2.3 Zero voltage switching in sub-resonant mode

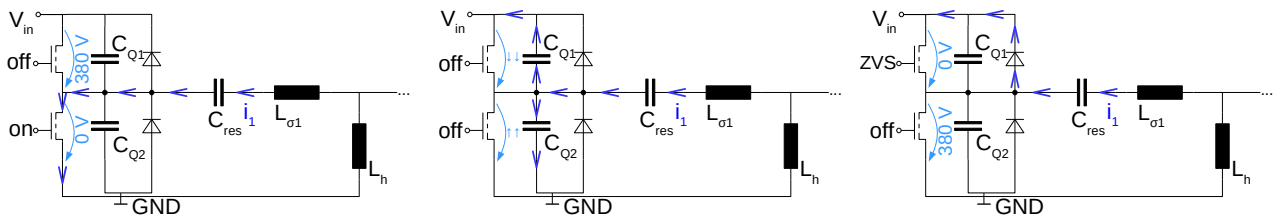


Figure 2.9.: Principal of zero voltage switching in case of the high transistor

Zero voltage switching (ZVS) means, that there is no voltage on a regarded transistor, when it switches on. On a half bridge the ZVS is generated by the cut-off current, that is still flowing through the transformer when both transistors are off. This current charges the parasitic capacitances. Usually such half

bridges are driven over-resonantly so that the transistor switches off before the output current becomes zero. Assuming that the parasitic capacitances $C_{Q1} \,||\, C_{Q2}$ are linear and much smaller than C_{res}, and neglecting the main inductance, this current can be written as:

$$i_1 = i_{\text{cut-off}} \cdot \cos\left(\frac{1}{\sqrt{L \cdot C}} \cdot t\right) \quad \text{where} \quad \begin{array}{rcl} C & = & C_{Q1} + C_{Q2} \\ L & = & L_{\sigma 1} + L'_{\sigma 2} \end{array} \tag{2.12}$$

The perfect dead time

$$t_{\text{dead}} = \frac{\pi \cdot \sqrt{L \cdot C}}{2} \tag{2.13}$$

here is 1/4 of the resonant period duration and ZVS occurs if

$$i_{\text{cut-off}} \cdot \sqrt{\frac{L}{C}} \geq V_{\text{in}} \tag{2.14}$$

A longer dead time causes the secondary rectifier to block and the current i_1 remains zero. If $i_{\text{cut-off}}$ is too low, ZVS is not possible. In some cases, hard switching of the complete input voltage can destroy the circuit because strong EMI inhibits the driver from working correctly. On the other hand, a too large cut-off current yields extreme steep signal slopes, strong EMI and higher losses, too.
The parasitic output capacitance ($C_{O(TR)}$) of the lateral HEMT devices is with 35 pF less than half as large as of comparable vertical power MOSFETs. The measurements 5.2 will show, that the total parasitic capacitance $C_{Q1} = C_{Q2}$ which also consists of the anti-parallel diodes D_{Q1} / D_{Q2} and the driver, is 110 pF, so if these diodes get removed in future projects, the capacity will reduce further. This makes ZVS in sub-resonant mode easy. In this case, the main inductance is not neglected, so a *significant* magnetizing current is still flowing, after the secondary rectifier turned off. This current $i_{\text{cut-off}}$ is here independent from the load and ensures ZVS even in open-loop condition (transient oscillation after power-on is not regarded). The resonant period of C and L is insufficiently long in this case and the dead time should not be 1/4 of this period but end after C are charged. A too long dead time could now even reverse the direction of i_1 as been shown in fig. 2.8. In true sub-resonant case, the parasitic capacitances C are charged after:

$$t_{\text{dead}} = \sqrt{L \cdot C} \cdot \operatorname{asin}\left(\frac{V_{\text{in}} \cdot \sqrt{C}}{i_{\text{cut-off}} \cdot \sqrt{L}}\right) \quad \text{while} \quad L = L_{\text{h}} + L_{\sigma 1} \tag{2.15}$$

2.4 Difference between SRC and LLC-converters

SRC and LLC-converters have the same resonant tank circuit consisting of one capacitor, one small inductor (usually the stray inductance) and one large inductor (usually the main inductance). In case of a SRC, the main inductance is much larger, than the stray inductance and is often assumed to be infinite. In this project, the main inductance is not neglected but consciously used for ZVS in sub-resonant mode. This behaviour does not automatically turn the circuit into an LLC. When both inductors are in same order of magnitude, the tank circuit can amplify the input voltage and its transfer function becomes significantly larger than 1 for a certain frequency band. This is the criterion for differing between SRC and LLC. [8]

3 Transformer

The transformer is one of the most important parts of the power supply. It is improbable to find a ready transformer on the market, that has correct inductances, winding ratios, size and current ratings. For this project, is is not necessary, to built an extremely small transformer, but it should be as thin as possible (max. 1 cm high). Therefore the decision of using an *EFD 30x15x9 core* was made. A toroidal core could also be possible, but is more difficult to design and to produce.
The design was made with GeckoMAGNETICS. There is no EFD-core in the database, so an ETD-Core with equivalent size was used. It was planned to built a core with 40 primary, 4 secondary windings and an air gap of 0.1 mm and to use a full bridge rectifier. But it pointed out, that the full bridge rectification would be very challenging. There are no ready-to-use rectifier drivers for full bridges, so normal gate drivers (including high gates) have to be used and the signals have to be made by using extra sensors or have to be taken from the primary side, which is difficult as well.
There is not enough space in the EFD-core for a centre-tapped transformer having 2x4 secondary windings. By reducing the number of windings to 31 primary and 2x3.2 secondary windings, the resistances of the wiring reduce and a lower number of strands can be used.
The winding ratio comes from the ability of using a PFC. If there is a boost converter in the PFC, the half bridge input voltage is $> 354\,V$. In the centre-tapped configuration, the DC output voltage is halve of the transformer's secondary side AC peak-to-peak voltage. Therefore, an half bridge input voltage of 377.8 V corresponds to the required 19.5 V output voltage. Without the PFC, the output voltage may be lower.
Available are two different litz wires:

- AWG 38, 40 x 0.1 mm
- AWG 41, 45 x 0.07 mm with extra insulation, 0.648 mm total diameter

The primary windings are made of the AWG 41, the secondary windings are made of 4 paralleled AWG 38 wires. It is difficult, to have interleaved windings.
When building the transformer with stacked secondary windings, the stray inductances are not equal. Placing the windings next to each other could be a solution, but with the coil former connectors on the upper and lower side, the only option of building a perfectly symmetric transformer is the point symmetric model (see fig. 3.1), which is not applicable for the PCB. Especially the secondary side rectifier would have to be symmetrical, too for this transformer. After testing several transformers including the stacked and the point symmetric one, the decision of using the stacked transformer is made and the PCB is designed to compensate the asymmetry.
The stacked transformer's height excluding the coil former is 11.17 mm (see fig. 3.2). The PCB is meant to be just 10 mm high. With perfect fitting windings, insulation material and a specially designed coil former, it should be possible, to build this transformer with 10 mm height.

Stacked winding model:

point symmetric winding model:

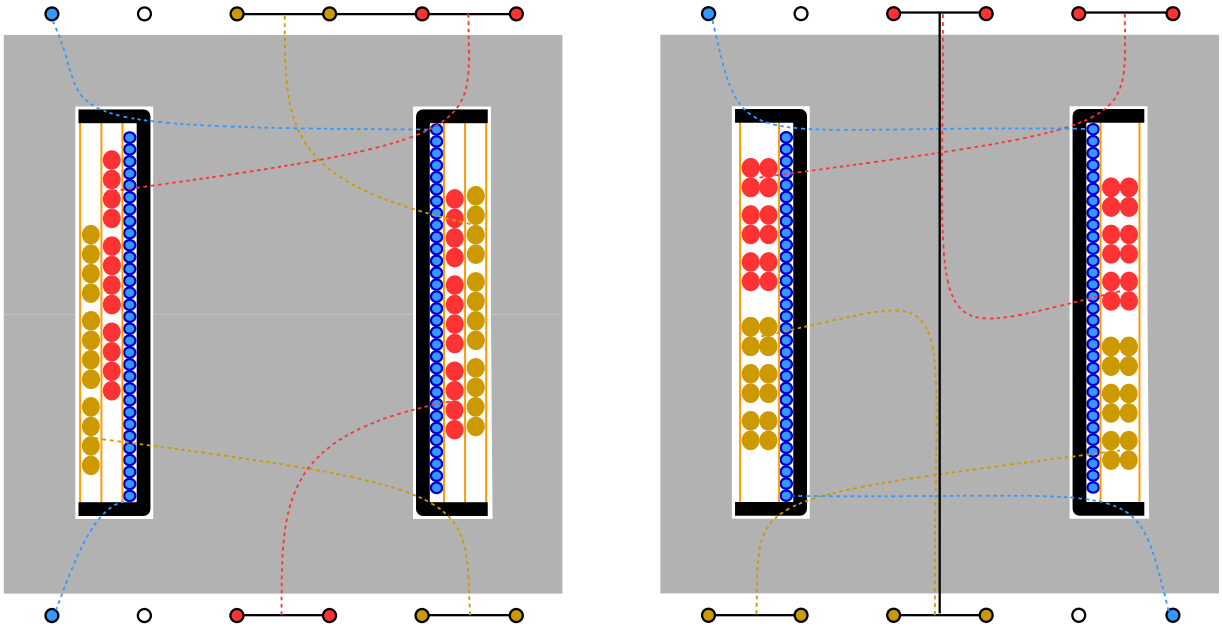
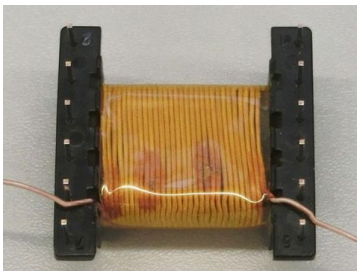
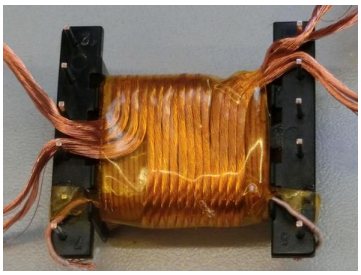


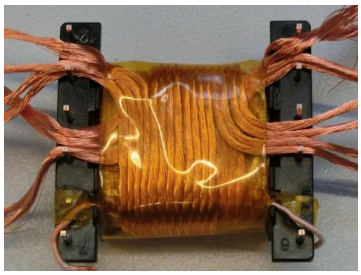
Figure 3.1.: Transformer winding models



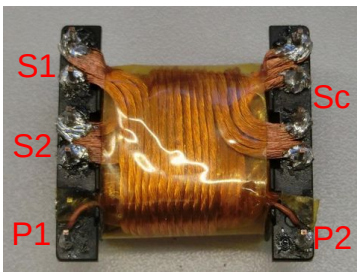
31 primary windings incl. insulation



3 + ~0.2 inner secondary windings

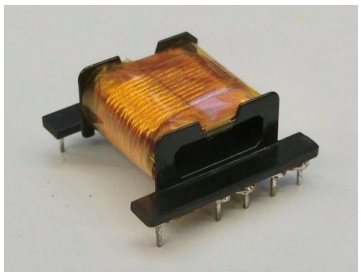


3 + ~0.2 outer secondary windings



soldered litz wires with corresponding designators

required transformer height



ready transformer without core

Figure 3.2.: Transformer building

Annotation: The mapping of designators of the physical transformer does not match the mapping of the circuit symbol. The primary and the inner secondary winding looks as being inversely arranged, but because of the mapping of designators, a positive current, that enters P1 corresponds to a positive current, that enters S2. Otherwise the connections in the schematic had to be intersected.

3.1 GeckoMAGNETICS Transformer calculation

With respect to the chosen core type (EFD), the given frequency and the available litz wires, there are not many options of building a more efficient transformer during this work. It pointed out, that it is the best to put as many primary windings as possible with one layer in the transformer.

There is no EFD-core type in GeckoMAGNETICS. ETD-cores with similar size parameters yield implausible results where either the inductance or the losses (temperatures) don't fit the measurements. For the Gecko-simulation, an EE-core was used. The EE-core type is the most similar one to EFD. The most parameters are similar to the EFD-datasheet values. Only the outer width and height are changed to get the same cross-sectional area as with the EFD core (see figure 3.3). The difference here is a little longer average magnetic field path.

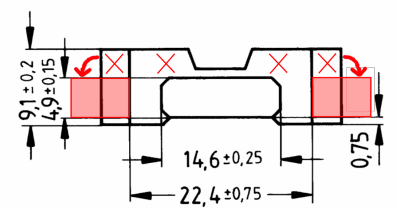


Figure 3.3.: EFD to EE core type (Image source: [1])

parameter	symbol	value
Height of one half	h	18.257 mm
Width	w	36.514 mm
Inner Width	wi	22.4 mm
Mid-leg Width	wm	14.6 mm
Length	l	4.9 mm
Air Gap Size	gap	0.117 mm
Windor Height	hw	11.08 mm

Table 3.1.: GeckoMAGNETICS core parameters

The air gap is not exactly known from the data sheet, but with the chosen gap, the main inductance fits the measured value (5.1). The four paralleled AWG 38 windings having 4x 40 strands are replaced by one AWG 38 winding having 160 strands. The distances between the windings are chosen to fit the measured stray inductance. Because GeckoMAGNETICS cannot deal with the centre tap transformer, an ideal full bridge rectification is assumed for the simulation.

parameter	symbol	value
Winding Strategy		Vertical
Distance between primary and secondary winding(s)		0.1 mm
Bobbin Gap	wb	0.9 mm
Bobbin Height	hb	20.1 mm
Primary Winding Nr. of Turns		31
Primary Winding Total Diameter	d	0.64 mm
Primary Winding Strand Conductor Diameter	di	0.07 mm
Primary Winding Number of Strands	n	45
Primary Winding Wire Spacing	yd	0 mm
Secondary Winding Nr. of Turns		3
Secondary Winding Total Diameter	d	1.48 mm
Secondary Winding Strand Conductor Diameter	di	0.1 mm
Secondary Winding Number of Strands	n	160
Secondary Winding Wire Spacing	yd	3.442 mm

Table 3.2.: GeckoMAGNETICS winding parameters

3.2 Calculated transformer efficiency

The power losses in the transformer can be classified in three categories:

- **Core losses** consisting of hysteresis losses and induced eddy currents.
- **AC conduction** in the following meaning the ohmic resistance including the skin effect. At high frequencies, the magnetic field of the current shifts the current towards the surface of the conductor. By using litz wires, the diameter of each strand shrinks and the effective conductor thickness increases. [6]
- **Proximity effect** is the same physical phenomenon as the skin effect, but it is not the self field of the current but an external magnetic field, that shifts the current, for example the stray inductance flux or a part of the main inductance field, that spreads around the air gap. [6]

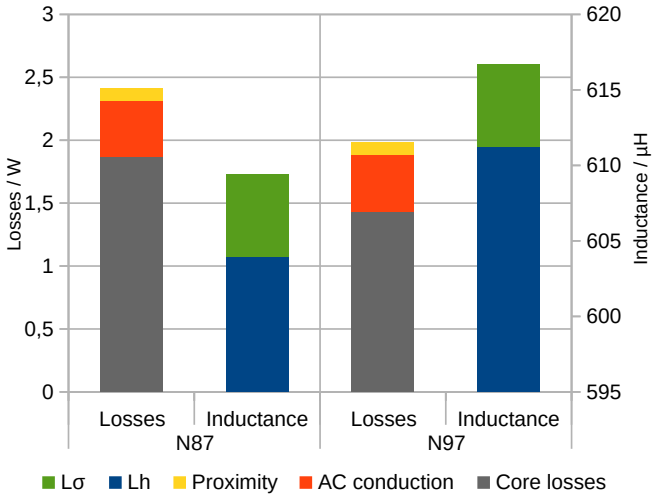


Figure 3.4.: Comparison of core materials (T: 25°C, gap: 0.117 mm, f:182.81 kHz)

There are still a lot of parameters, for example core material, temperature, air gap modification or frequency, that influence the efficiency of the transformer. Figure 3.4 shows, that the N97 core material is the preferred one for this project. The cost of the core is negligible in comparison with i.e. the HEMT devices. There is no gapped N97 core on the market. It may become difficult to produce a defined gap in the range of 0.1 mm with un-gapped cores, so in this project, the N87 cores are used.

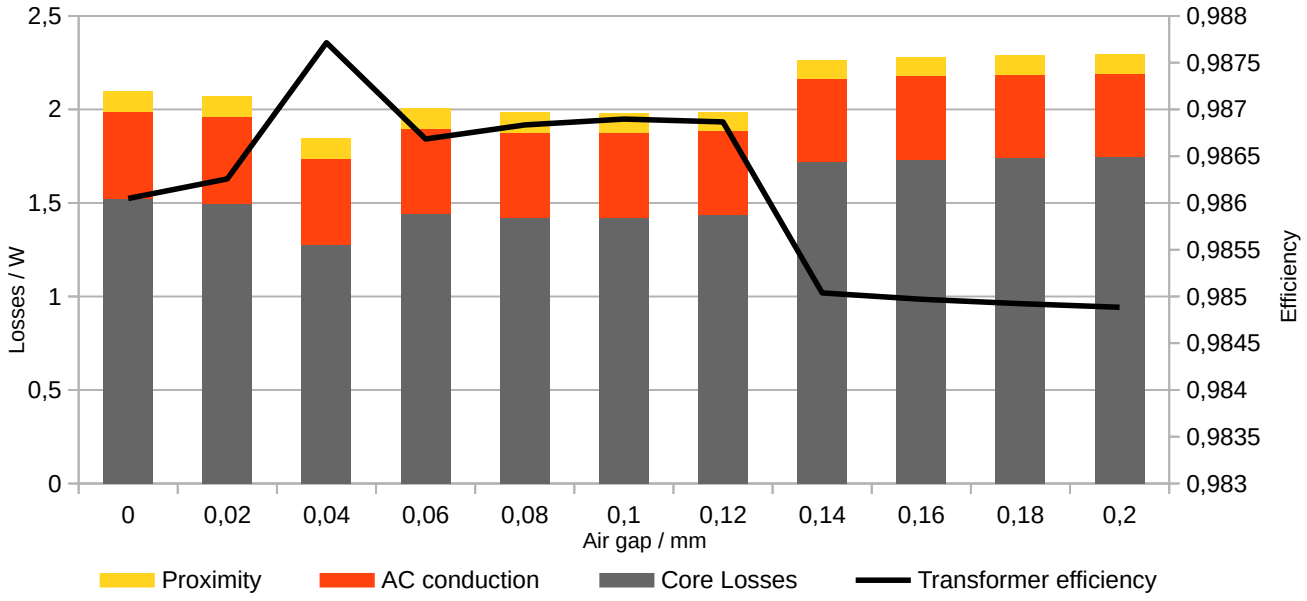


Figure 3.5.: Transformer losses depending on air gap (Material: N97, T: 25°C, f:182.81 kHz)

Figure 3.5 shows, that the air gap has not big influence on the transformer efficiency. So if a way for building fixed air gaps using the un-gapped core halves is found, the gap can be freely chosen to get a targeted main inductance.

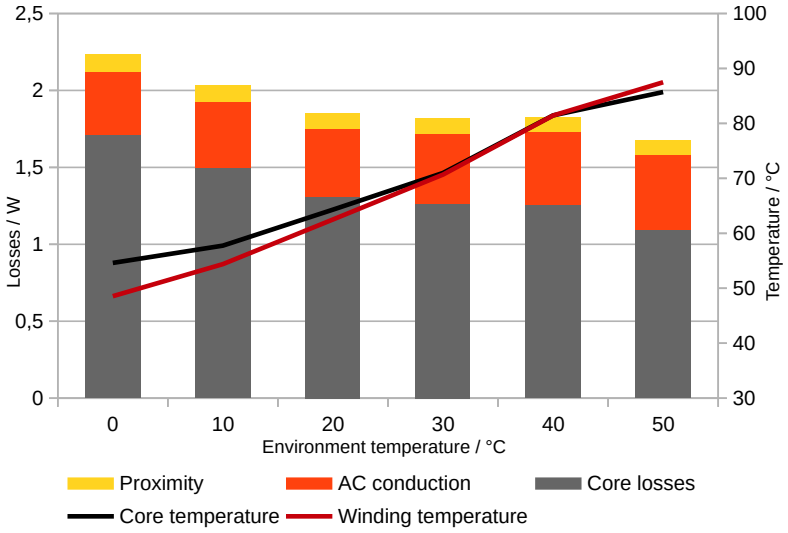


Figure 3.6.: Transformer losses depending on the environment temperature (Material: N97, gap: 0.117 mm, f:182.81 kHz)

Figure 3.6 shows, that the core material becomes more efficient at higher temperatures. This is a benefit as it helps to prevent overheating. For the temperature calculation, the bottom side of the transformer is assumed to be thermically insulated. The other sites are passively air cooled.

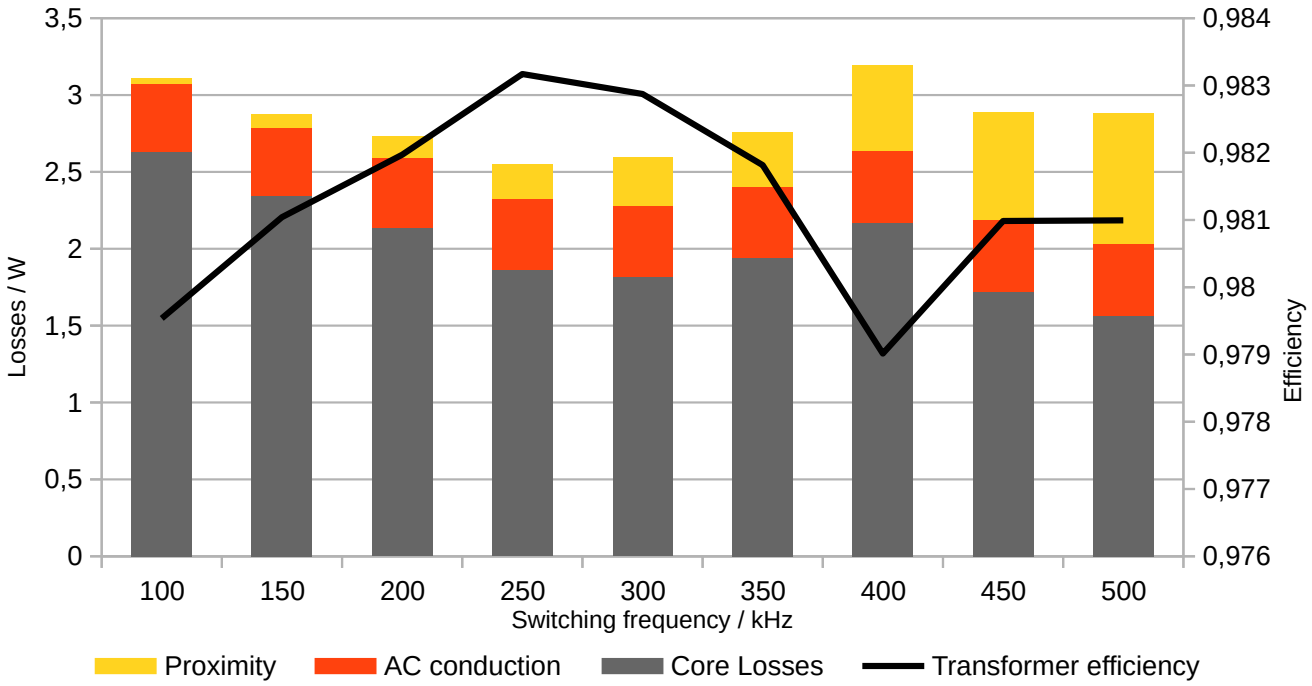


Figure 3.7.: Transformer losses depending on frequency; C_{res} adjusted (Material: N97, T: 25°C, gap: 0.117 mm)

Figgure 3.7 shows, that this core will work better at higher frequencies - especially if the litz wire types get adapted for higher frequencies.

4 PCB development

This chapter focuses on the PCB development with the transformer from chapter 3. Figure 4.4 is an overview of the complete topology.

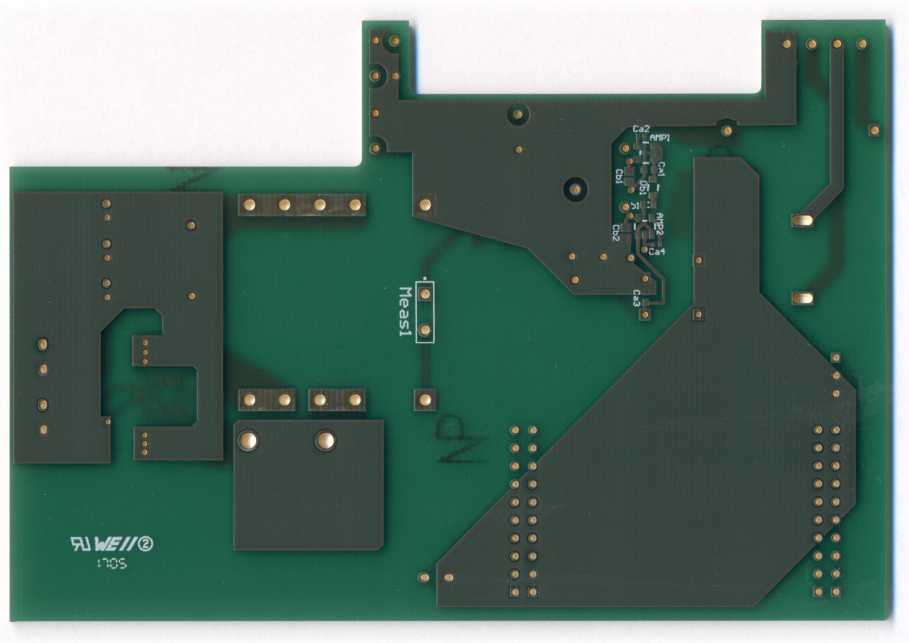


Figure 4.1.: bottom side of the un-soldered PCB

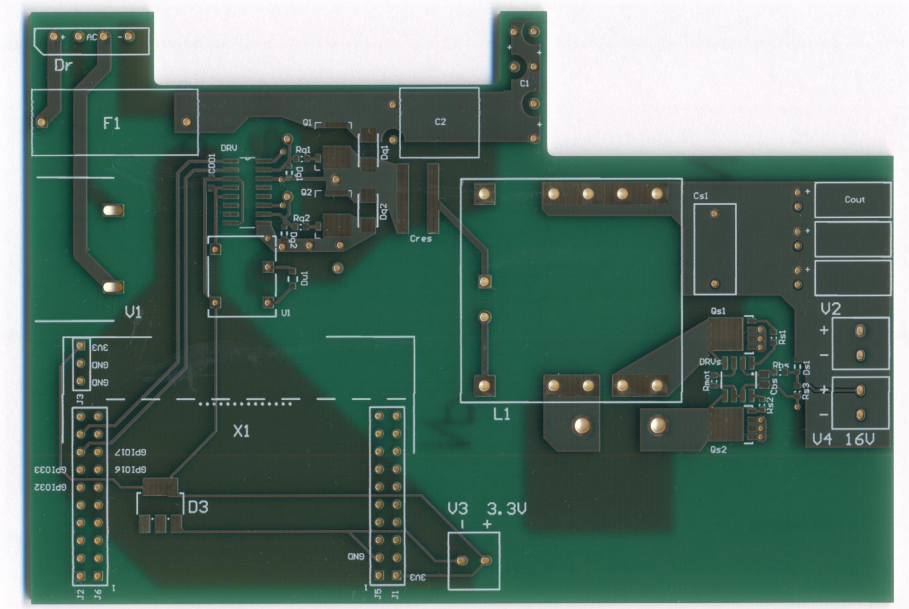


Figure 4.2.: top side of the un-soldered PCB

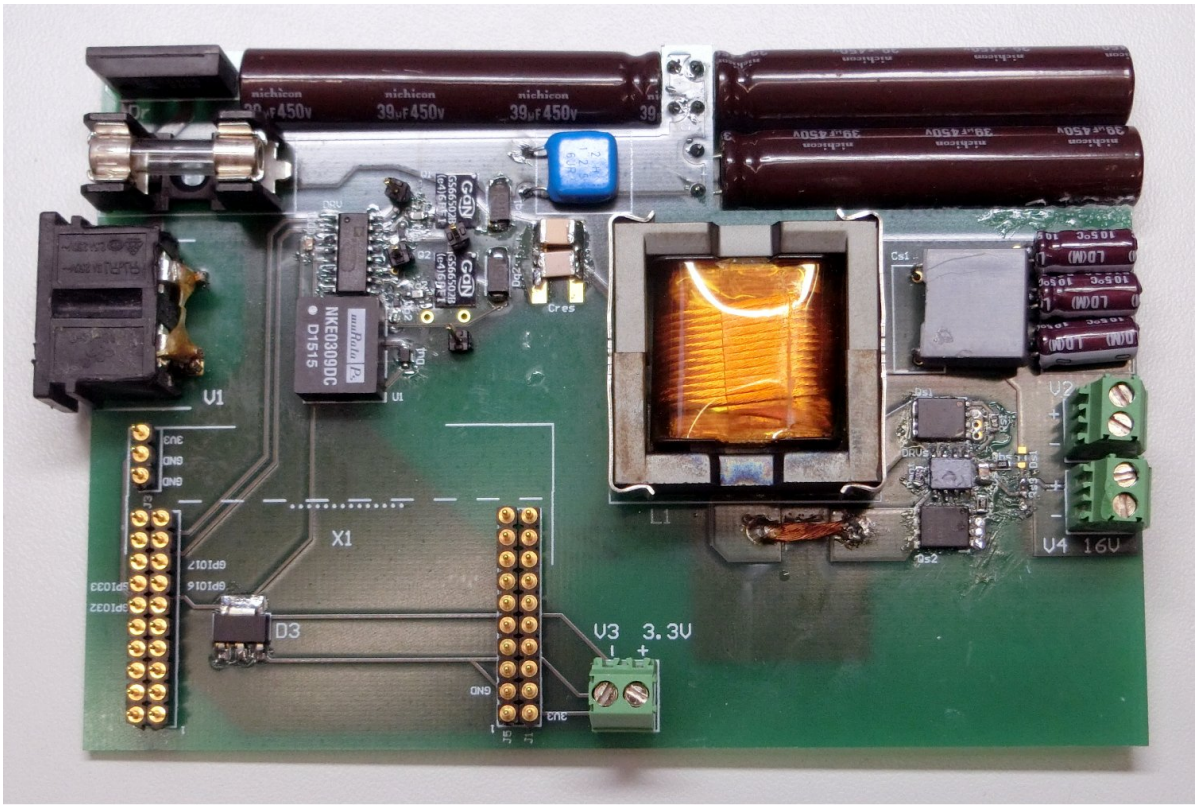


Figure 4.3.: final PCB (revision #4)

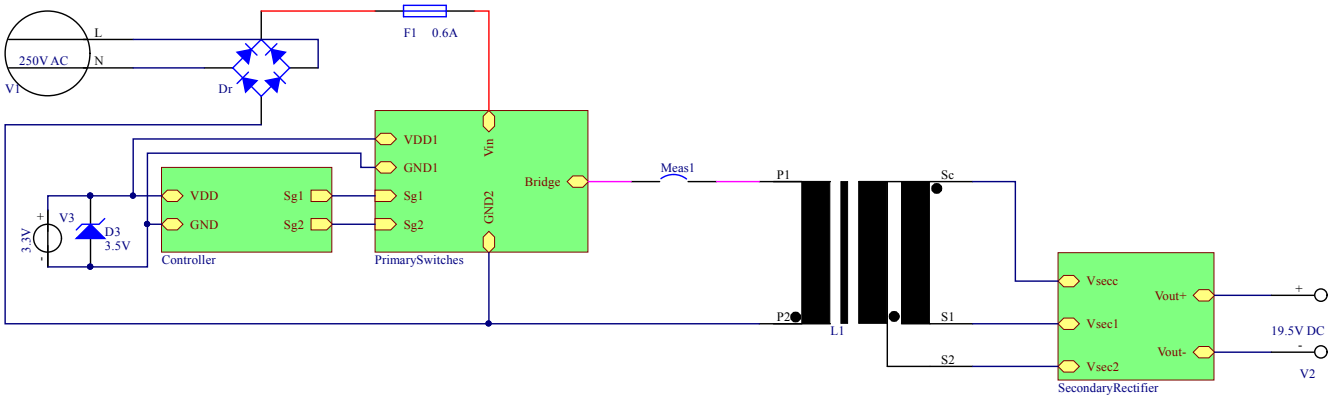


Figure 4.4.: General SRC scematic

4.1 PCB current paths

The parasitic inductances especially on the secondary side are not totally negligible. The area within the current paths should be small for low EMI emission.

The outer secondary winding is promised to have a larger stray inductance. So this winding is connected to Q_{s1} (blue path). In the red path there is an auxiliary, small air inductor which can be modified for adjusting the exact stray inductance of the inner winding. It is not only the inductance, that influences the current pulse, but also the different inner winding's resistance, due to the smaller scope and shorter wire strands. It turned out, that it is better, to bypass this air inductor directly and use the duty cycle for

getting equal current pulses. When actively rectifying, even a small deviation in the currents can cause non-continuous rectification: The output capacitor gets overcharged in one switching state with high current and there will be no current for a couple of ongoing cycles. Read section 4.4.1 for details.

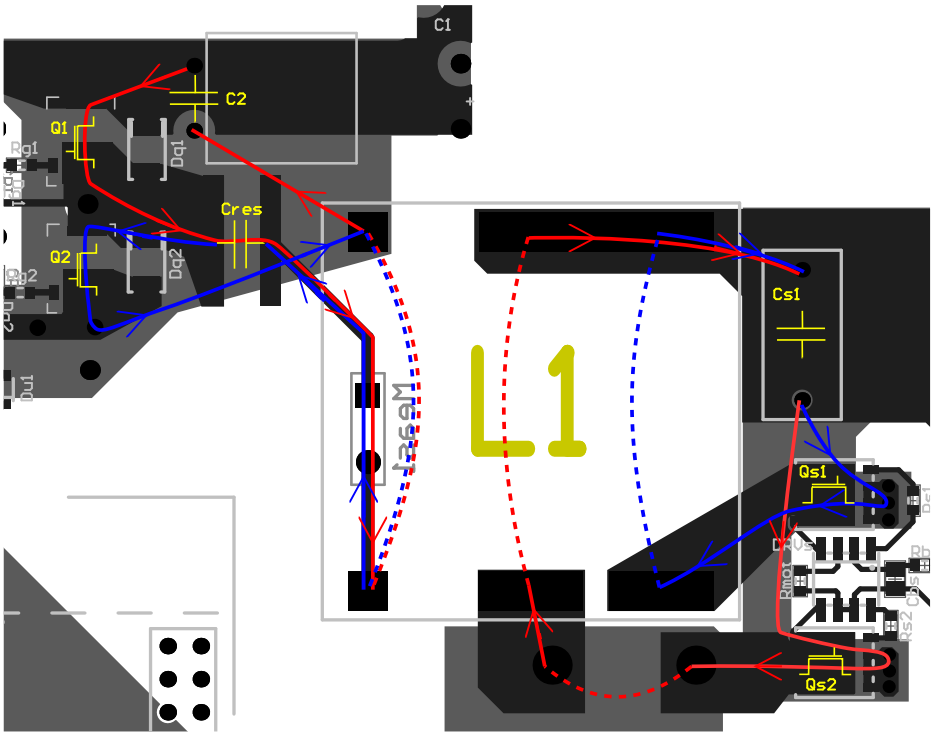


Figure 4.5.: PCB high-frequent current paths

4.1.1 Auxiliary air inductor

There is a break in the connection for the inner secondary winding. To connect over this break, a strand of litz wire can be used and create a defined stray inductance and resistance. The problem with this air inductor is the increase of EMI. The measurements pointed out, that it is possible to control the symmetry of the current pulses by adjusting the duty cycle, and that this air inductor is not necessary. So it was shorted since revision #3.

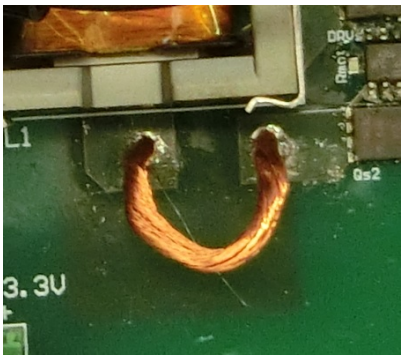


Figure 4.6.: Air inductor (revision #2)

It seems, that the perfect duty cycle depends on the input voltage. The duty cycle for revision #2 was optimized for 60 V to get active rectification (see section 4.4.1) in each half period as early as possible. But at 200 V revision #2 produced significant deviations in the current pulses. So for revision #3, the duty cycle was optimized for the targeted 380 V.

The principle behind the duty cycle control is, that the average voltage on L_h must be zero. Due to the capacitor C_{res}, the system is self-balanced. If the average during one period is not zero, C_{res} gets charged or de-charged until there is a steady state, again. The voltage-time area under a short pulse must be as

large as the area under a long pulse. Therefore the peak voltage of the shorter pulse becomes higher. The peak voltages must have equal values to load the secondary buffer capacitors in each half period. The larger this buffer capacitors are, the more precise the duty cycle has to be adjusted. The final duty cycle for PCB-revision #3 and higher is set to 0.506, so the asymmetry is quite small.

4.2 Primary switching circuit

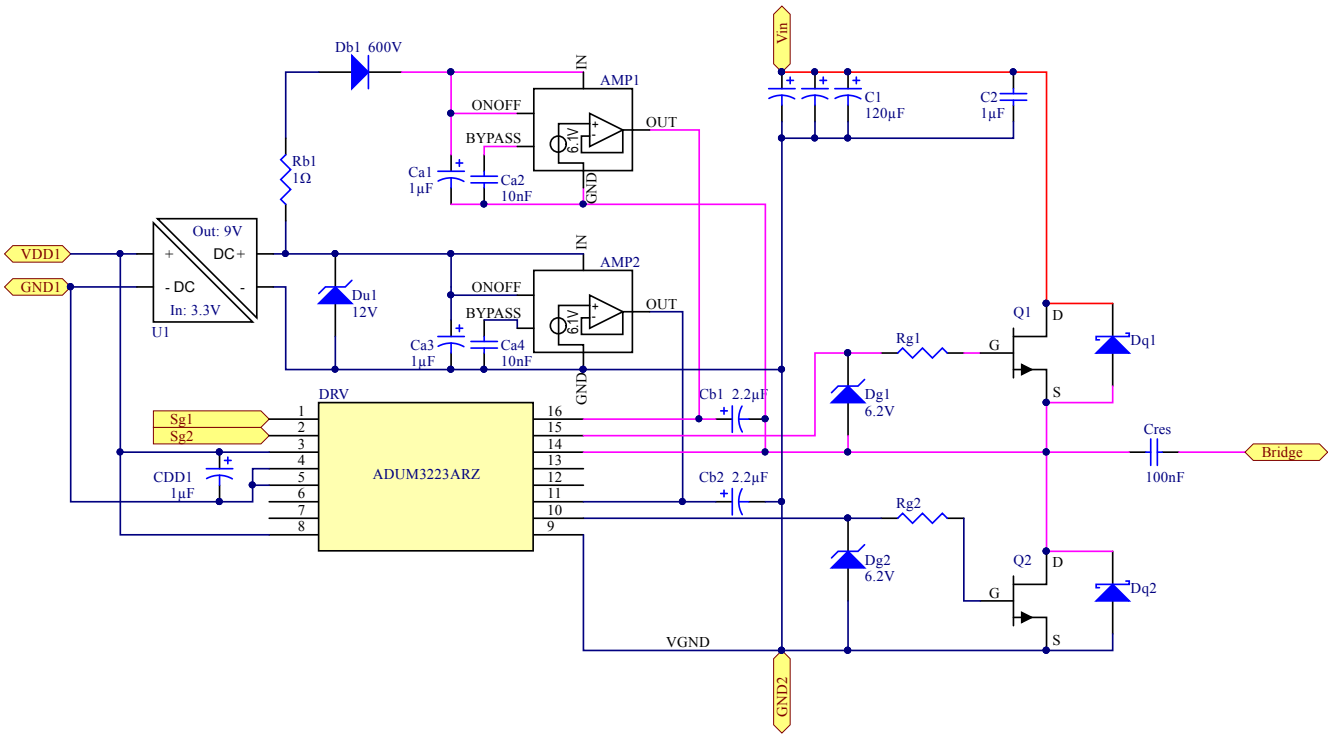


Figure 4.7.: Primary switching circuit

For the primary side switching, new GaN-E-HEMTs where used. High Electron Mobility Transistors have no body diode. The behaviour of HEMTs is comparable with JFETs, while this GaN Systems **e**nhancement mode HEMT devices are self-blocking. Because of the lack of a body diode, HEMTs can principally block voltages in both directions. When short-circuiting gate and drain, the transistor blocks in reverse direction, but of course not the full voltage, which required a dual gate device. [5] Short-circuiting gate and source, as like in this half bridge topology while the transistor is off, yields a behaviour like a normal MOSFET. When the source-drain-voltage exceeds the threshold voltage, the transistor becomes conductive by its channel. Therefore the reverse voltage on the HEMT is not 0.7 V but the gate threshold voltage. An anti-parallel diode is not required, but in this prototype, anti-parallel Schottky diodes where used as a precaution.

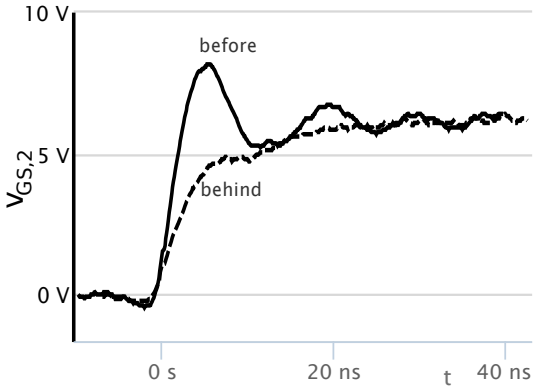
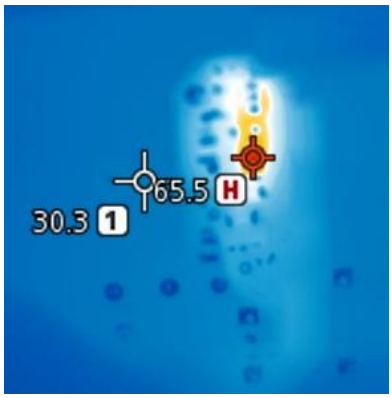


Figure 4.8.: Q_2 - gate turn on

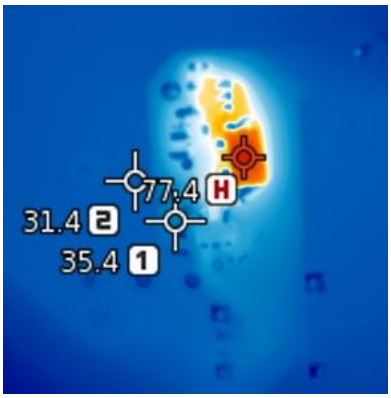
The transistors need a gate voltage between 5 and 7 volts, can be damaged with voltages higher than 10 volts. It is not that easy, to drive this transistors. The voltage loss of the bootstrap diode is not negligible and there are not many voltage converters for 6 or 7 volts on the market. Therefore a 9 V converter and two linear controllers are used to generate 6.1 V for the gate signals. The high-gate controller is behind the bootstrap diode and changes its voltage potential together with the bridge. The gate drive circuit is mainly taken from the manufacturer's recommendation paper. [2]
The gate signals are measured between driver and gate resistor. At this point, there is a certain ringing, which gets filtered out by the gate resistor as been shown in fig 4.8. There is still some latitude for reducing the gate resistor.

4.2.1 Boot diode failure

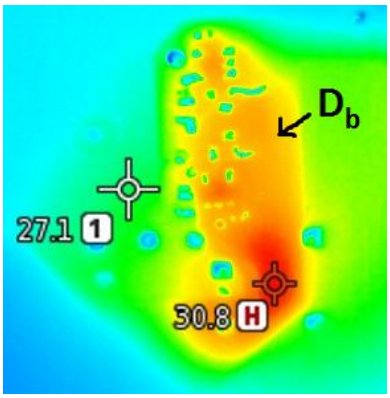
Revision #2 of the PCB broke at an input voltage of abut 250 V. The bootstrap diode D_b was destroyed (conductive) afterwards, the voltage regulators on the lower side (AMP_1, AMP_2) and the surrounding capacitors were defective as well as the driver, and the high-transistor had a gate-source short-cut. It is implausible, that this short-cut was the trigger of this failure, because this wouldn't have destroyed the boot diode. Supposedly this diode overheated due to reverse-recovery losses. On the rebuilt board (revision #3), this diode and two alternatives were watched with an infra-red camera:



RRE02VSM6S standard recovery diode at 200 V



MRA4005T1G standard recovery diode at 50 V



RFN2L6STE25 super fast recovery Schottky-diode at 50 V

Figure 4.9.: Heat-up of different diodes

It can be seen, that at least a fast recovery diode is required. There is no such diode for the selected package, so the footprint has to be changed in future revisions. For this project, the RFN2L6STE25 (same as the transistor anti-parallel diodes) is taken and soldered next to the designated footprint.

4.3 Controller

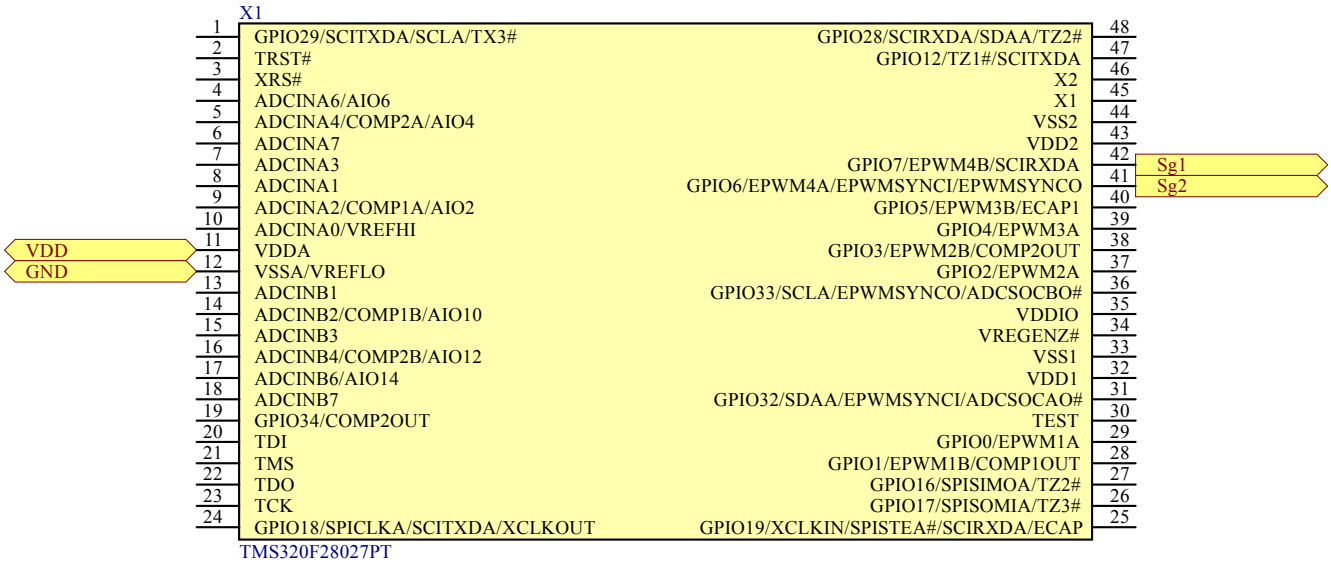


Figure 4.10.: Controller connections

The controller is a Texas Instruments Piccolo launchpad, which generates the gate signals for the primary switches by using the HRPWM-port 4.

4.4 Secondary Rectifier

For active rectification an automatic driver IC is used:

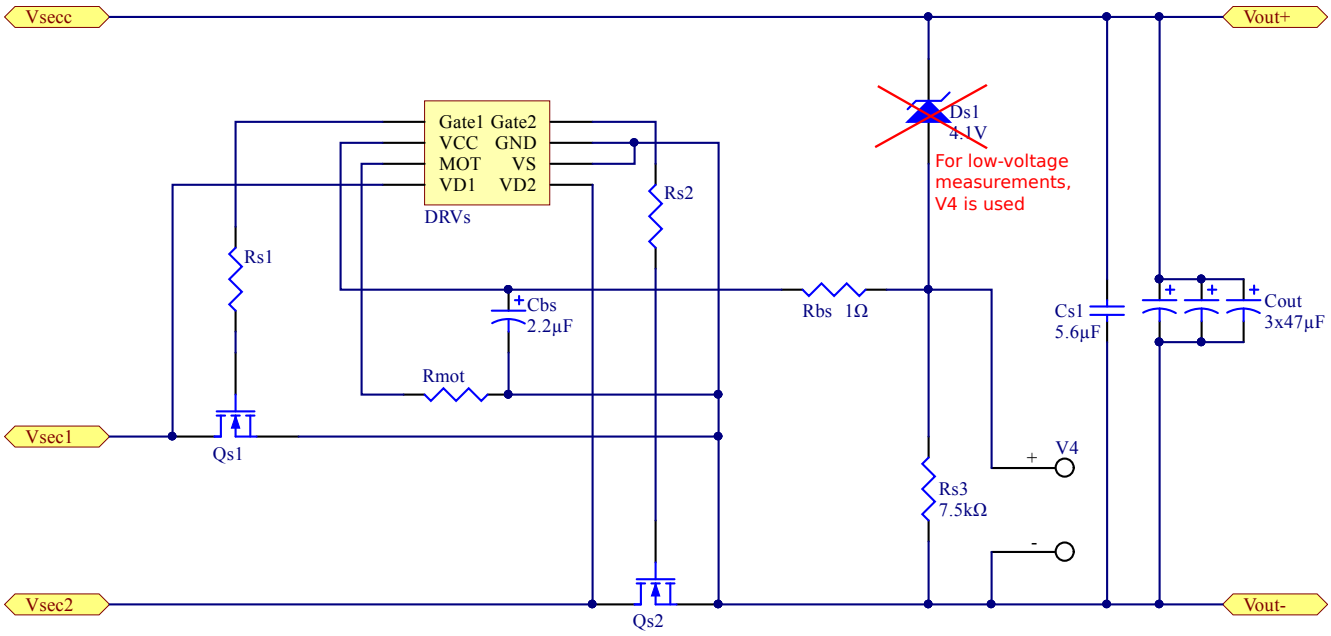


Figure 4.11.: Secondary, active rectifier

It generates the gate signals automatically by measuring the transistor's drain-source-voltage. The transistors are placed in the ground-side of the circuit, which prevents from driving high gates. The transistors best work with a voltage of 16 V. The diode D_{s1} subtracts 4.1 V from the 19.5 V output. The body diodes of the transistors will provide a working but inefficient rectification even without the driver. Therefore, the circuit can start up by itself and starts active rectification when a sufficient output voltage is reached. For low voltage measurements, D_{s1} is left out and the driver is provided with external voltage.

4.4.1 Non-continuous rectification

The first measurements showed, that the rectifier is not generating gate signals in each half period. According to the data sheet [4] the R_{MOT} of 51 kΩ belongs to a Minimum On Time (MOT) of 1.06 µs, which is longer than the delay between the current pulses. The duration of this delay depends on the difference between the resonant frequency and the switching frequency. In consequence, R_{MOT} was reduced to 27 kΩ which did not completely solve the problem with non-continuous rectification.

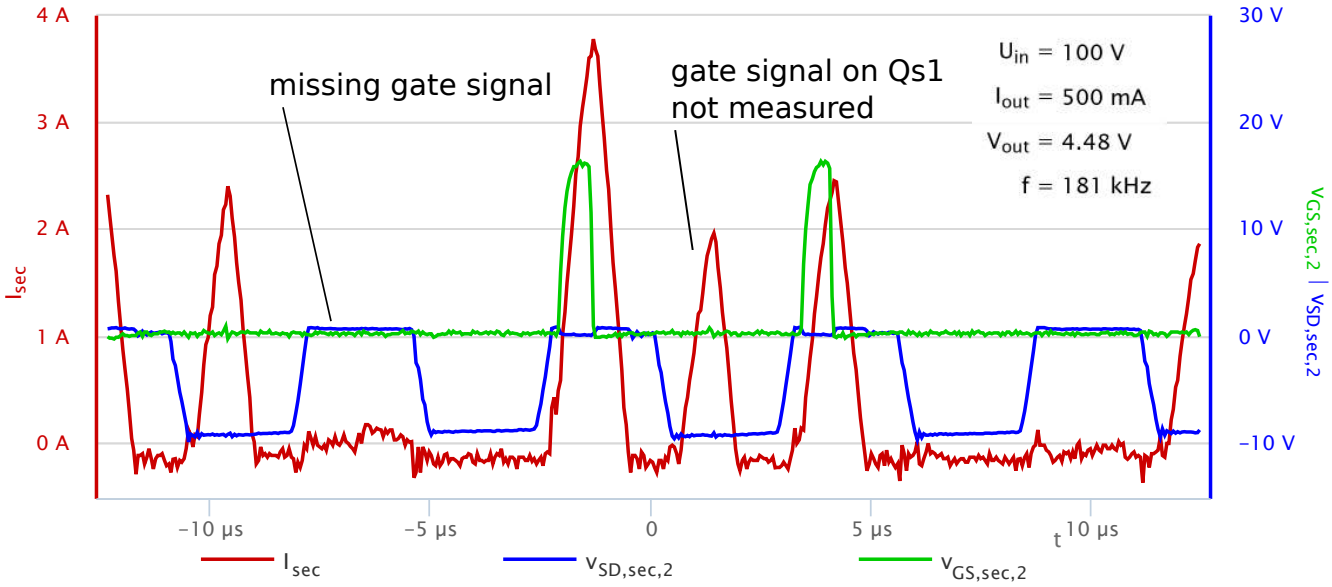


Figure 4.12.: Non-continuous rectification

The driver begins to generate gate pulses for all half periods since the output current becomes higher than about 3 A. This threshold can be reduced to 2.5 A by adjusting the duty cycle as described in section 4.1.1 but this doesn't even fix the problem. Without a minimum load, there isn't a current in every half period. The body diode threshold voltage of 0.8 V prevents current from flowing in non-actively rectified half periods. Figure 4.12 shows a small current even in one of the non-actively rectified half periods. This causes a body diode forward voltage > 0.7 V during the complete half period. It is unclear, why the driver is not generating a gate pulse here. It may also depend on the early turn off problem described in the following section.

4.4.2 Early turn off problem

Even with high output currents and/or -voltages, the active rectifier doesn't keep the transistor on for the complete half period but turns off immediately after the current maximum. According to the active rectifier design notes [3], this bug is caused by parasitic inductances in the transistor. With an $R_{DS,on}$ of just 1.2 mΩ, several amperes are required for the resistive on-voltage to be higher than the driver's turn-off threshold (V_{TH1}) of about 4 mV. The parasitic inductance of the device adds an additional voltage drop having the same sign as the resistive voltage drop for increasing current but reduces the absolute on-voltage for decreasing current. This is the reason why the driver turns the gate off after the current maximum.

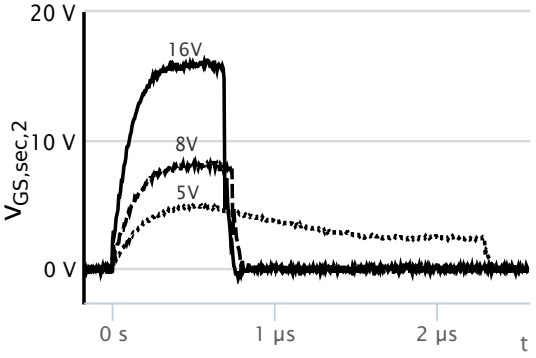


Figure 4.13.: Early turn off fix for 1.2 A output current

There are not many possibilities to reduce the parasitic inductance for the PG-TDSON-8 - package. The only option is, to increase the on-resistance, for example by reducing the driver's supply voltage. With less than 6 V supply voltage, the driver starts to do active rectification till the ending of the half period. Before the final turn-off, the gate voltage gets reduced further, to enable the driver detecting the remaining voltage drop for low currents. Figure 4.13 shows the gate signal for different supply voltages.
Weather such an automatic, active rectification can provide enough stability and efficiency for this project or if i.e. rectification signals from the primary controller are necessary should be subject of future work. The BSC014N03LS MOSFET was chosen for rectifier power losses less than 0.2 W. While it seems that the gate drive for this transistors produces even higher losses, smaller transistors should be chosen for future work. With the early turn off problem, the rectifier produces the highest losses over the complete power supply, which can be seen in the infra-red pictures in section 5.3.

5 Measurements

For the measurements, the PCB is provided with DC-voltage, because AC-voltage would cause a certain swing in the converter's input (V_{C1}), which disturbed the measurements. Input voltage, output voltage and output current are measured by using multimeters (Fluke 87V), the signal curves are measured with two digital oscilloscopes (Tektronix TDS 2024B) having synchronous trigger.
On the primary side four 1:10-probes measure the voltages to the primary side ground. The gate signals are measured between driver and gate resistor. There is a certain swing in this signals, that will not be behind the gate resistor as been shown in fig. 4.8.
On the secondary side, three differential 1:10-probes (TT-SI-9001) for voltage measurement and one Rogowski coil (CWT PEM Rogowski Current Waveform Transducer) for current measurement are used. The Rogowski coil cannot measure DC, but the DC-part of the current should be equal with the output current through the multimeter. With this information, the original i_{sec} leaving the centre-tapped transformer clamp can be reconstructed.

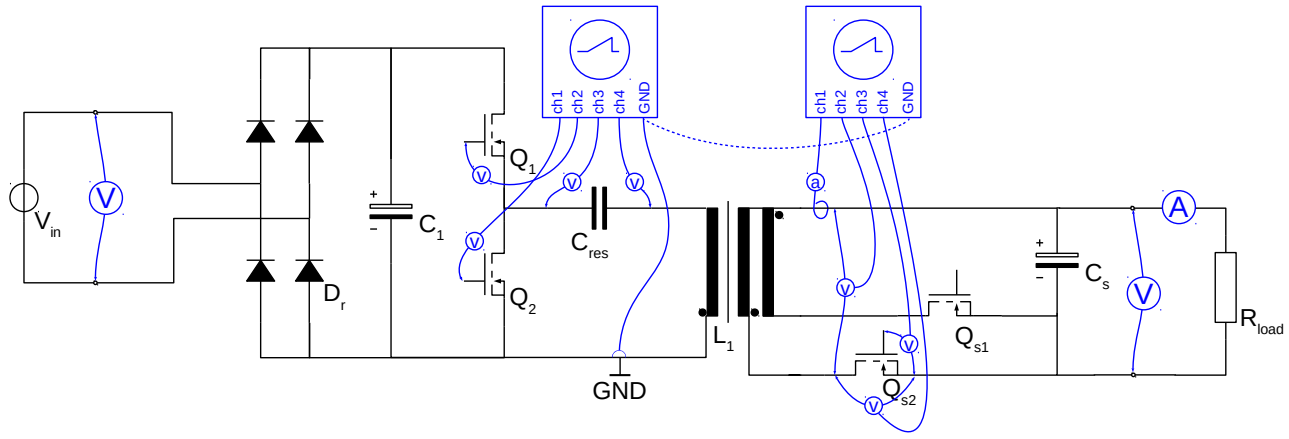


Figure 5.1.: Measurement connections

5.1 Revisions

Several modifications have been applied to the PCB since the first set-up:

- **Revision #1**: Basic prototype according to circuit plan.
- **Revision #2**: R_{MOT} adjusted to 28 kΩ as a solution for the non-continuous rectification bug. Duty cycle of the controller optimized for getting equal current pulses at 60 V.
- **Revision #3**: Complete rebuild of PCB (two empty PCBs were ordered) after damage through the D_b-failure 4.2.1. R_{b1}, R_{bs} reduced to 0 Ω. D_b replaced with RFN2L6STE25 Schottky diode. C_{res} set

to $33 + 47\,\text{nF}$. Auxiliary air inductor removed (directly connected). Duty cycle of the controller optimized for getting equal current pulses at 380 V.

- **Revision #4**: R_{s1} and R_{s2} set to $0\,\Omega$ because the $1\,\Omega$-resistors have been damaged by re-soldering for gate signal measurement. This modification should have no significant influence on the circuit.
- **Revision #5**: Transformer core replaced by 1x N87 gapped + 1x N97 un-gapped. Untested revision.

Check the part list in section A.2 for more details.

5.2 Comparison of simulation and measurement

A lot of parameters regarding the real device are not known. The parasitic capacitances C_{Q1}, and C_{Q2} cannot even be measured. But the complete signal curves of simulation and measurement can be compared. Using the analytic program developed in chapter 2, it is easy to play with the parameters until the signal looks like the measurement. The following parameters are found and used:

parameter	value for analytic program	value for geckoCIRCUITS
C_{res}	80 nF (known Capacitor value)	80 nF
C_{Q1}	110 pF	110 pF
C_{Q2}	110 pF	110 pF
L_h	$604\,\mu$H	$604\,\mu$H
$L_{\sigma 1}$	$2.7325\,\mu$H	$5.465\,\mu$H
$L^*_{\sigma 2}$	$2.7325\,\mu$H	0 H
R_2	$10\,\text{m}\Omega$	$10\,\text{m}\Omega$
I_{out}	8.17 A	8.17 A
t_{on}	$2.32\,\mu s$	$2.32\,\mu s$
t_{dead}	415 ns	415 ns

Annotation: $\tau = \frac{1}{f_s} = 2 \cdot t_{on} + 2 \cdot t_{dead}$

Table 5.1.: Simulation parameters

According to the manufacturer's data sheet [1], the transformer should have a main inductance of $L_h = N^2 \cdot \Lambda_L = 31^2 \cdot 315\,\text{nH} = 303\,\mu\text{H}$ but the simulated signal best matches the measured signal with nearly the double value. A raw, inaccurate measurement using a HP 4276A LCZ meter also gives values between 600 and $630\,\mu$H, so this value is taken. Because GeckoMAGNETICS cannot deal with a secondary stray inductance, there is only the primary stray inductance with double value in the GeckoCIRCUITS simulation.

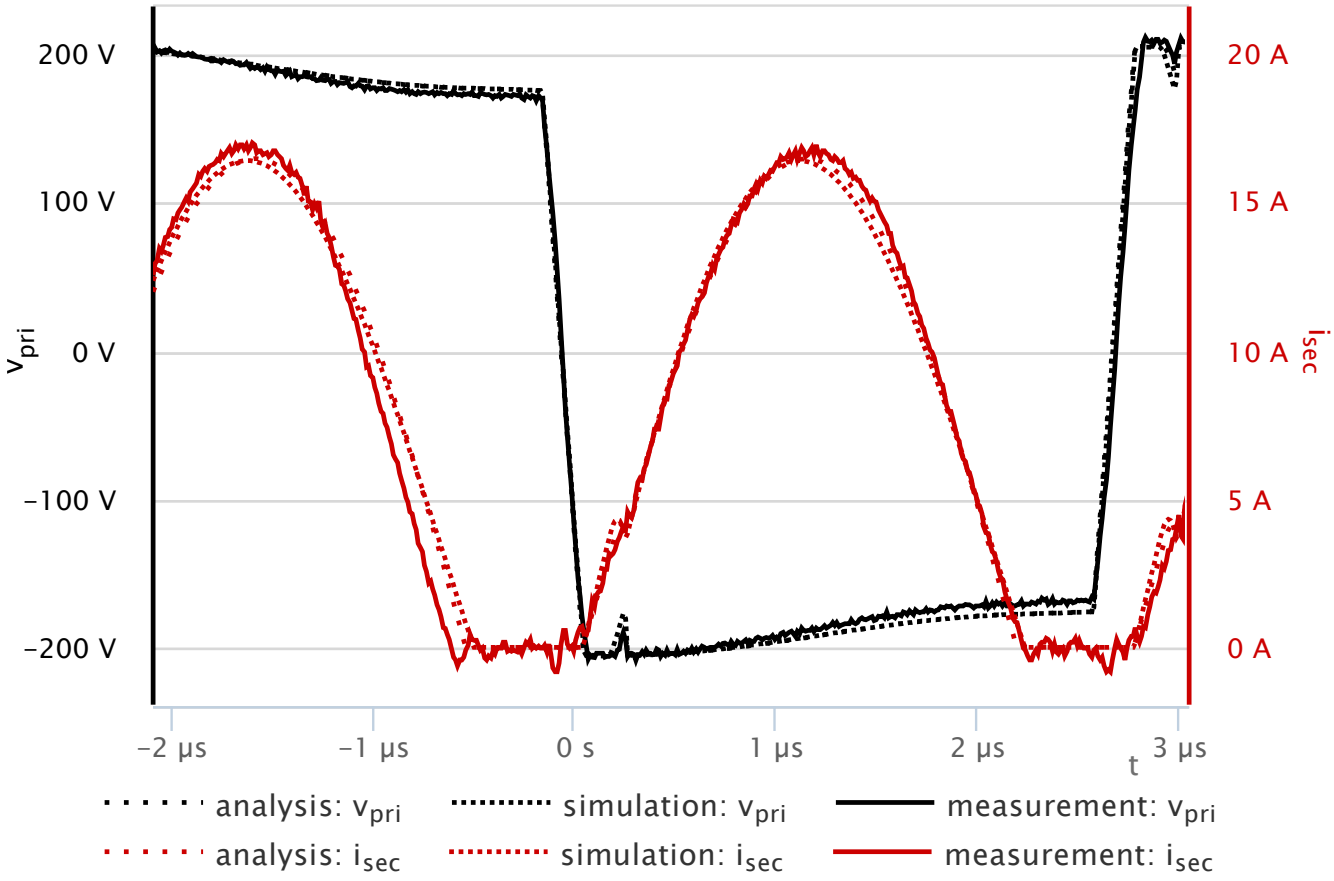


Figure 5.2.: Comparison of analytic program, GeckoCIRCUITS simulation, and measurement (revision #3)

5.3 Signals and infra-red assessment

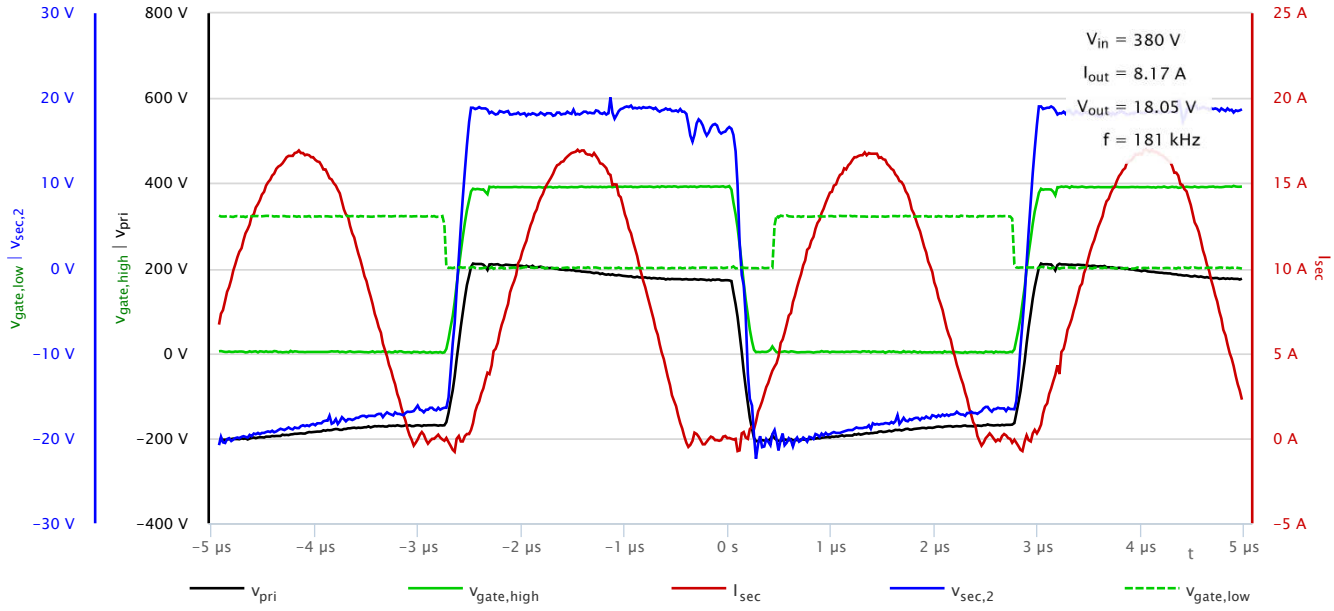
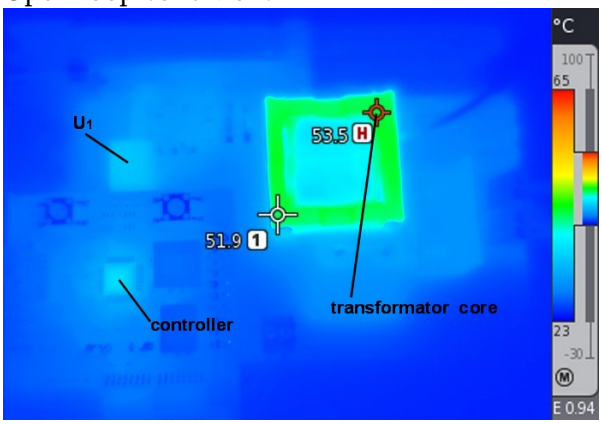


Figure 5.3.: Final measurement at 380 V (revision #4)

Open loop condition:



Heavy load condition (8 A):

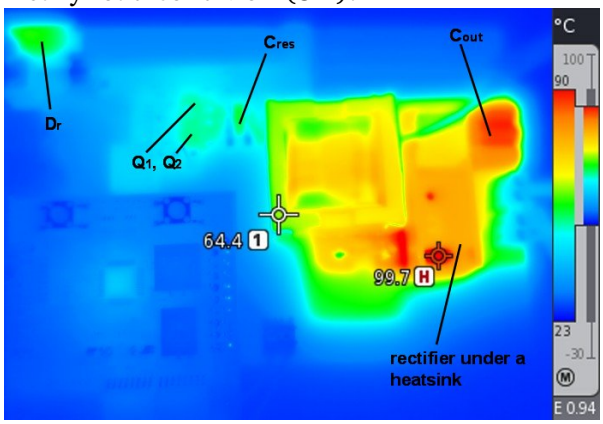


Figure 5.4.: Infra red picture of working power supply

Under open loop condition, there are only some driver losses and the core magnetisation. Under heavy load, the secondary rectifier, which still had the early turn off problem in this measurement, produces the highest losses. But the transformer and the output capacitor are becoming non-satisfyingly warm, too. A measurement of the current through C_{s2} shows, that there is a significant current flowing through this capacitor, but clearly not enough to relieve C_{out}. The output capacitors should get reinforced for future work. The sub-resonant switching tends to be higher stress for these capacitors than over-resonant switching would be. Maybe it makes sense to switch to over-resonant switching for heavy loads.

5.4 Conclusion

The primary switching circuit works and seems to be highly efficient. A smaller DC/DC-converter can be used on the primary side. A small fast recovery diode is required for D_b. The project pointed out, that the secondary side with high currents can quickly become the bottleneck of a low voltage, high-frequent SMPS. For getting higher transformer efficiencies, the increase of the switching frequency should be intended. The primary side is designed for much higher frequencies. On the secondary side, the rectification is expected to become challenging - hopefully with smaller transistors and higher $R_{DS,on}$, the automatic rectifier driver could be kept. With the actual efficiency, the device cannot work under full load.

The next tasks for developing a complete power supply will be the design of a control strategy together with the PFC and the self-supply of the controller infrastructure. The analytic program, that was developed during this project, can be extended to help calculating and evaluating control functions.

A Appendix

A.1 Program documentation

The program is written with Object Pascal (FPC/Lazarus). Unit1.pas contains the GUI together with unit1.lfm. PolynomUtil and Graph2D maintain some tools for calculating with polynomial or general functions and plotting them on a chart. The SRC-Simulation is done in the functions.pas.
The TSRCValues class contains all required functions and subclasses. One instance of TSRCValues represents a time interval that includes no switching transitions. There is no class, that represents *one* SRC-Simulation. All Methods and Variables, that belong to the complete simulation, are implemented as global class procedures / variables. So the TSRCValues-Class itself (not its instances) represent the total simulation and it is therefore not possible, to create for example two different SRC simulations/circuits in one program. For future work, a real "SRCCircuit"-Class should be created.
The TSRCValues-Class is inherited by two different subclasses: TDOpen and TDShort. The TDOpen contains the differential equations for all states when the secondary side rectifier is blocking, TDShort when it is conducting. All relevant parameters and the next switching transition are calculated in the doUpdate functions.
The construction of the signal curves then works as follows:

- Decide weather the simulation starts with open or shorted rectifier
- Create one TSRC-Values-instance (TDOpen or TDShort)
- Set the boundary condition parameters Vcres_0, Vq2_0, Ih_0, I2_0 and t_offset.
- Call doUpdate
- after doUpdate, the nextState and endTime-parameters hold all necessary information for creating the following state.
- The state is now able to be plotted on a chart. Each state internally starts with $t = 0$, t_offset shifts the signals to their correct time position, i.e. the endTime of the previous state. The TPFunction-class can plot hard-coded functions with respect to the t_offset on a chart.

The class procedure TSRCValues.update manages the creation of a state chain, that is one period long. This chain is stored in the TSRCValues.period-array. When re-creating the chain, for example because the input voltage has changed, doUpdate on the first state must be called again. If the nextState-parameter then does not fit the existing next state, destroy this state and re-create it. This task is done in TSRC-Values.checkState. The boundary conditions of the first state (startup values) are taken from the class variables Vcres_0_def, Ih_0_def, I2_0_def.
Calling TSRCValues.update several times and setting the last state's ending values as the next startup

values means going to the stationary state. This process can be accelerated by calculating the average current through L_h during one period and subtract it from Ih_0_def.
Until now, the calculation represents a system with fixed output voltage but the basic setup of the SRC without control strategies has no fixed output voltage. Maybe a fixed output current can be taken and the program should find the output voltage, that belongs to this current. At this voltage the average of I_2 should resemble the taken output current. The TSRCValues.gotoSteadyState function provides this approximation for fixed output voltage or fixed output charge. Set the parameter, that is not fixed to -1. Because there is no control strategy yet, fixed output voltage *and* - current are not possible.
At last some hints to the IDE: Lazarus provides several compilation modi, in this case for 32 bit platforms, 64 bit platforms and for debug 32 bit. For being able to debug the program, this debug mod has to be selected. The used PolynomUtil unit contains some new/experimental Object Pascal code structures, which have still bugs in the FPC compiler. As one effect, modifications on this unit may be ignored when just clicking the run-Button. Use start ⇒ re-compile after changing this unit.

A.2 part list

qty.	mfr.	part number	corr. circuit el.	description
2	EPCOS	B66423G0000X197	L1	EFD 30x15x9 N97 ungapped core (#5)
1	EPCOS	B66423G0000X187	L1	EFD 30x15x9 N87 ungapped core (#1-#4)
1	EPCOS	B66423U0315K187	L1	EFD 30x15x9 N87 gapped core
1	EPCOS	B66424W1012D001	L1	Coil former
2	EPCOS	B66424B2000X000	L1	Yoke
1	AD	ADUM3223ARZ	DRV	primary gate driver
1	Infi.	IR11688S	DRVs	secondary rectifier driver
1	Schurt.	4300.0097	S1	IEC 60320-1 C7 power connector
1	Schurt.	0031.8211	F1	fuse holder (don't forget the fuses :-)
1	Murata	NKE0309DC	U1	3.3 to 9V DC/DV-converter
2	TI	LP2985IM5-6.1	AMP1, AMP2	6.1V voltage controller
1	TI	LAUNCHXL-F28027	X1	piccolo launchpad
2	Molex	90131-0765	X1	piccolo launchpad socket (2*10 Pins)
1	TE-Conn	640454-3	X1	piccolo launchpad socket (1*3 Pins)
3	TE-Conn	284391-2	V2, V3, V4	DC-clamps
0	TE-Conn	1-2129458-1	V2	10 A thin output jack for future work
2	GaN-Sys	GS66502B	Q1, Q2	650 V HEMT
2	Infi.	BSC014N03LS G	Qs1, Qs2	30 V rectifying transistors
1	Recton	RS105	Dr	Primary 50 Hz Rectifier
1	NXP	BZV90-C3V3,115	D3	3.5V security diode
3	Rohm	RFN2L6STE25	Dq1, Dq2, Db	flyback diodes and Db since (#3)

1	Rohm	RRE02VSM6S	Db	Boot Diode (#1-#2)
2	Rohm	EDZVT2R6.2B	Dg1,Dg2	6.2 V gate protection diodes
1	Rohm	UDZVTE-1712B	Du1	12 V voltage regulation diode
1	Rohm	TFZGTR3.9B	Ds1	Secondary driver voltage regulation diode
2	Wurth	885012205050	Ca2, Ca4	10 nF bypass class 2 ceramic capacitors
3	Wurth	885012207079	Cb1, Cb2, Cbs	2.2 μF boot ceramic capacitors
3	Wurth	885012206076	Ca1, Ca3, CDD1	1 μF ceramic capacitor
1	UC-C	KTD501B125M76A0T00	C2	1.2 μF ceramic capacitor
1	Kemet	C1812W333KBRACTU	Cres	33 nF resonance ceramic cap. (#3-#5)
1	Kemet	C1812C473KBRACAUTO	Cres	47 nF resonance ceramic cap. (#3-#5)
1	Kemet	C1808V104KBRACTU	Cres	100 nF resonance ceramic cap. (#1-#2)
1	Kemet	R60CF4560506AK	Cs1	5.6 μF film capacitor
3	Nichi.	ULD1E470MDD1TD	Cout	47 μF output electrolytic capacitor
3	Nichi.	UCS2W390MND9	C1	39 μF 50 Hz buffer electrolytic capacitor
4	Yaego	RC0603FR-070RL	Rb1, Rbs, Rs1, Rs2	boot / gate resistors (#3/#4-#5)
2	Rohm	ESR03EZPJ1R0	Rb1, Rbs	1 Ω boot resistors (#1-#2)
1	Rohm	ESR03EZPJ822	Rs3	8.2 kΩ voltage regulation resistor
1	Rohm	ESR03EZPJ513	Rmot	51 kΩ MOT-resistor (#1)
1	Rohm	ESR03EZPF2702	Rmot	27 kΩ MOT-resistor (#2-#5)
2	Rohm	ESR03EZPJ2R0	Rs1, Rs2	2 Ω gate resistors (#1-#3)
2	Rohm	ESR03EZPJ430	Rg1, Rg2	43 Ω gate resistors

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